

Digital Techniques (313303)

MSBTE Diploma · K-Scheme · Model Question Paper — Set C

Time: 3 Hours**Max. Marks: 70****Instructions:**

1. All questions are compulsory.
2. Answer each next main question on a new page.
3. Illustrate your answers with neat sketches wherever necessary.
4. Figures to the right indicate full marks.
5. Assume suitable data, if necessary.
6. Use of non-programmable electronic pocket calculator is permissible.
7. Mobile phone, pager and any other electronic communication devices are not permissible in the examination hall.

Q.1 Attempt any FIVE of the following:**10**

- a) Convert $(10110.101)_2$ into its decimal equivalent.
- b) List any four AND laws of Boolean algebra.
- c) Convert $Y = AB + \overline{A}C$ into standard (canonical) SOP form.
- d) Draw the logic diagram of clocked D flip-flop using NAND gates and write its truth table.
- e) Define resolution of a DAC. Find the resolution of an 8-bit DAC whose full-scale output is 10 V.
- f) Write the expressions for difference and borrow of a half subtractor and draw its logic diagram.
- g) State any two differences between combinational and sequential logic circuits.

Q.2 Attempt any THREE of the following:**12**

- a) Perform the following using 2's complement method: i) $(58)_{10} - (23)_{10}$ ii) $(23)_{10} - (58)_{10}$
- b) State De Morgan's theorems. Using them, simplify $Y = \overline{\overline{AB} + \overline{C}}$ and verify the result with a truth table.
- c) Explain 4 : 1 multiplexer with block diagram, truth table, Boolean expression and logic diagram.
- d) Draw and explain a 4-bit SIPO shift register using D flip-flops. Draw its timing diagram for serial data 1101.

Q.3 Attempt any THREE of the following:**12**

- a) Minimize using K-map and draw the logic diagram: $F(A, B, C, D) = \sum m(1, 3, 7, 11, 15) + d(0, 2, 5)$

- b) Realize the EX-OR function $Y = \overline{A}B + A\overline{B}$ using only NAND gates. Write the output of each gate.
- c) Compare weighted resistor DAC and R-2R ladder DAC. (Any four points)
- d) Draw and explain a 4-bit twisted ring (Johnson) counter using D flip-flops with its truth table and waveforms.

Q.4 Attempt any THREE of the following:

12

- a) Convert the following:
 - i) $(2F9.A)_{16} = (?)_2 = (?)_8$ ii) $(0.6875)_{10} = (?)_2$ iii) $(1001\ 0110)_{BCD} = (?)_{10} = (?)_{16}$
- b) Describe a 4-bit universal shift register with its block diagram and mode control table.
- c) Explain T flip-flop (using J-K flip-flop) with logic diagram, truth table and excitation table. Give one application.
- d) Compare EPROM and Flash memory. (Any four points)
- e) Design a 3 : 8 line decoder. Write its truth table and draw the logic diagram.

Q.5 Attempt any TWO of the following:

12

- a) Obtain the minimal POS form of $F(A, B, C, D) = \prod M(0, 2, 3, 8, 9, 10, 11, 13)$ using K-map and realize it using NOR gates only.
- b) Draw the logic diagram of J-K flip-flop and write its truth table and excitation table. Explain the race-around condition and the methods to avoid it.
- c) Design a MOD-12 asynchronous counter using J-K flip-flops. Write its truth table and draw the timing diagram.

Q.6 Attempt any TWO of the following:

12

- a) i) Design an 8 : 1 multiplexer using 4 : 1 and 2 : 1 multiplexers.
ii) Implement $F(A, B, C) = \sum m(1, 3, 5, 6)$ using a 4 : 1 multiplexer.
- b) How does a Solid State Drive (SSD) store data? Draw its block diagram, describe its main parts and list its features.
- c) Design a full subtractor using K-map. Write its truth table and draw the logic diagram.

Note: This is a **model question paper prepared by Ananda Technologies** only for practice and exam preparation, based on the pattern of previous MSBTE question papers and the K-scheme syllabus. It is **not an official MSBTE paper**, and it does **not** mean that these questions will come in the exam. Answers follow standard textbook points; marks shown are indicative. Free for students — anandatechnologies.in