

Fundamentals of Power Electronics (313335)

MSBTE K-Scheme · EE Sem III · Model Question Paper — Set A · Model Answers

Answers are written point-wise as expected in MSBTE model answers. Marks scheme lines in blue italics are indicative. All waveforms are plotted from the circuit equations and all numerical values were calculated by program.

Q.1

a) Advantages of power electronic systems

2 M

1. **High efficiency** — devices work as switches (fully ON / fully OFF), so power loss is very small (efficiency 95–99 %).
2. **Small size and less weight** compared with motor-generator sets, magnetic amplifiers, rheostats.
3. **Fast response** — switching in microseconds, so control is quick and precise.
4. **No moving parts** — long life, silent operation and very little maintenance.

(Any four, ½ M each)

b) Symbols of SCR, TRIAC, DIAC and IGBT

2 M

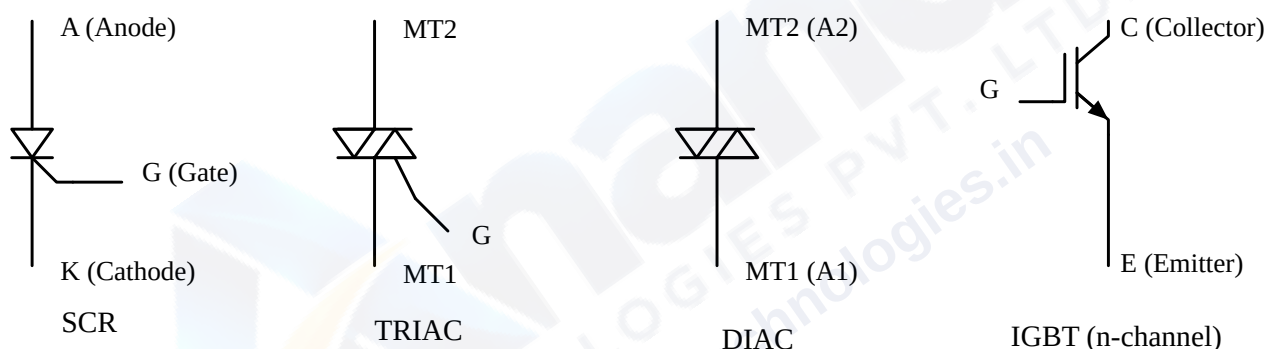


Fig.: Symbols of SCR, TRIAC, DIAC and IGBT

(½ M each symbol with terminals)

c) Latching current and holding current

2 M

i) **Latching current (I_L)**: It is the minimum anode current which must flow through the SCR just after it is triggered (gate signal removed) so that it remains in the ON state.

ii) **Holding current (I_H)**: It is the minimum anode current below which the SCR turns OFF from the ON (conducting) state. $I_L > I_H$.

(1 M each)

d) Turn-ON methods of SCR

2 M

1. **Forward voltage triggering** — V_{AK} increased above breakover voltage V_{BO}
2. **Gate triggering** — positive gate current applied (most common and reliable method)
3. **dv/dt triggering** — fast rising anode voltage; charging current of junction capacitance turns it ON

4. **Thermal (temperature) triggering** — high junction temperature increases leakage current

5. **Light triggering** — light falling on the junction (LASCR)

(Any four, $\frac{1}{2}$ M each)

e) Firing angle and conduction angle

2 M

Firing angle (α): It is the angle measured from the instant the SCR becomes forward biased (zero crossing of supply for a single phase circuit) to the instant at which the gate pulse is applied and the SCR starts conducting.

Conduction angle (β or θ_c): It is the angle (in a half cycle) for which the SCR remains in the conducting state. For R load, conduction angle = $\pi - \alpha$.

(1 M each)

f) Duty cycle and chopping frequency

2 M

Chopping period $T = T_{ON} + T_{OFF} = 3 + 1 = 4$ ms

Duty cycle $D = T_{ON}/T = 3/4 = 0.75$ (i.e. 75 %)

Chopping frequency $f = 1/T = 1/(4 \times 10^{-3}) = 250$ Hz

(Duty cycle 1 M, frequency 1 M)

g) Applications of PV cell

2 M

- Solar street lights, garden lights and traffic signals
- Solar water pumping for agriculture
- Roof-top solar power plants (grid connected / off-grid)
- Battery charging, calculators, watches; power supply in satellites

(Any two, 1 M each)

Q.2

a) Construction of IGBT

4 M

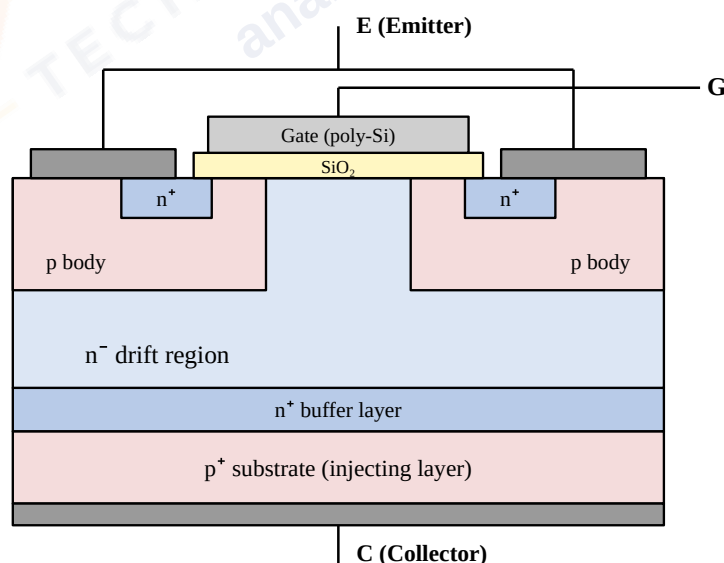


Fig.: Constructional details of IGBT

- IGBT is a **four-layer ($p^+ n^+ n^- p n^+$)** device with three terminals: **Collector (C)**, **Gate (G)** and **Emitter (E)**.
- Its construction is similar to a vertical power MOSFET, except that the n^+ drain substrate is replaced by a **p^+ substrate** called the **injecting layer**; the collector metal is attached to it.
- Above the p^+ layer is an **n^+ buffer layer** (in punch-through IGBT) and a lightly doped **n^- drift region** which blocks the forward voltage.
- **p body** regions are diffused into the drift region and **n^+ emitter** regions are diffused into the p body. The emitter metal touches both n^+ and p body (short).
- The **gate** (polysilicon) is insulated from the p body by a thin **SiO_2** layer, so the gate draws almost no current (high input impedance, like MOSFET).

(Labelled diagram 2 M, description 2 M)

b) RC triggering of SCR

4 M

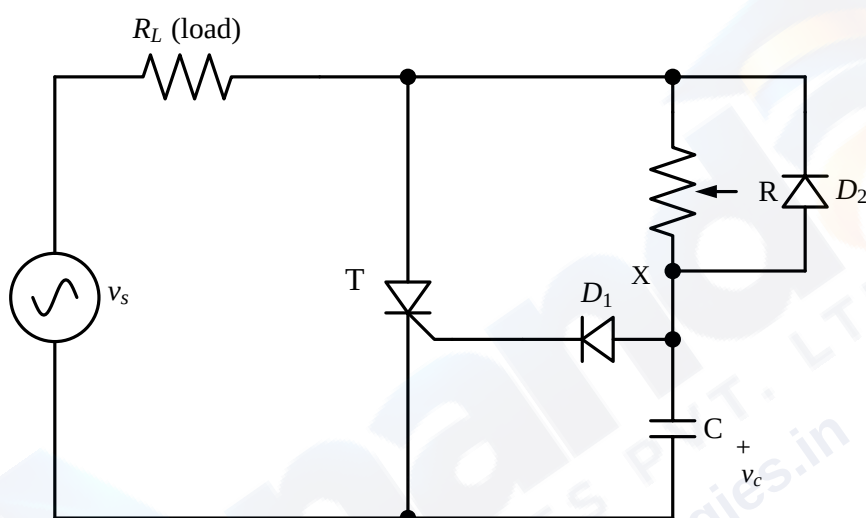


Fig.: RC half-wave firing circuit of SCR

- **Negative half cycle:** diode D_2 conducts and capacitor C charges to the negative peak $-V_m$ (lower plate positive). D_1 blocks reverse voltage to the gate.
- **Positive half cycle:** after the negative peak, C starts charging through R from $-V_m$ towards the positive supply voltage. The capacitor voltage lags the supply voltage.
- When v_c reaches the gate trigger voltage ($V_{gt} + \text{diode drop of } D_1$), gate current flows through D_1 and the **SCR fires**. After this the SCR voltage falls to ≈ 1 V and C stops charging.
- Increasing R (time constant RC) delays the instant at which v_c reaches V_{gt} , so α increases. Because of the RC phase shift, **α can be varied from about 0° to nearly 180°** .
- For reliable firing RC is chosen such that $RC \geq 1.3 (T/2)$, where T is the supply period.

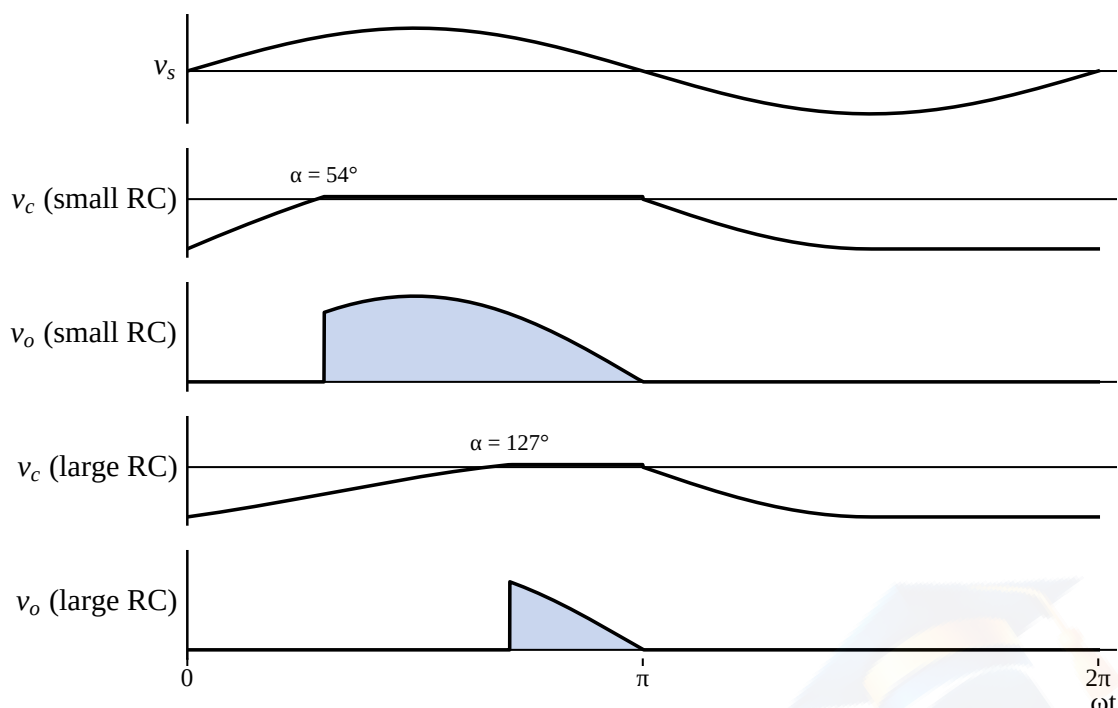


Fig.: Waveforms of RC half-wave firing circuit — α can be varied beyond 90° (up to nearly 180°)

Plotted example: small RC $\rightarrow \alpha \approx 54^\circ$, large RC $\rightarrow \alpha \approx 127^\circ$ (beyond 90° , not possible with R firing).

(Circuit 1 M, waveforms 1 M, explanation 2 M)

c) Class A commutation

4 M

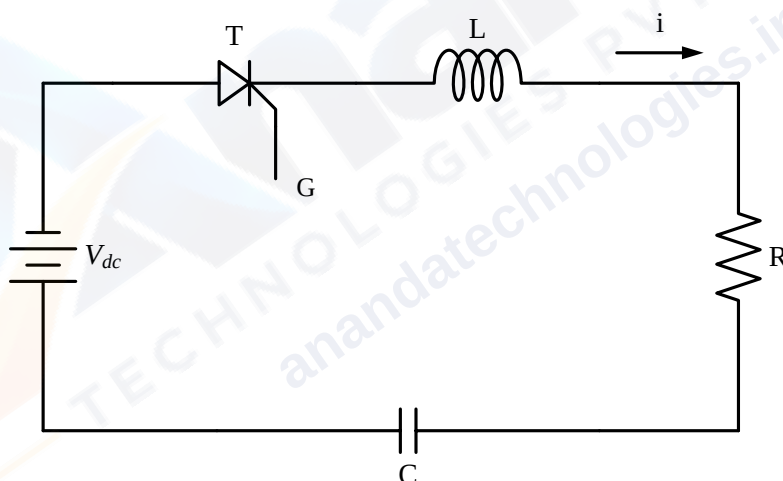


Fig.: Class A (resonant / load) commutation circuit

- Class A is also called **self commutation**, **load commutation** or **resonant commutation**.
- An inductor L and capacitor C are connected with the load so that the circuit is **under-damped** (for series R-L-C: $R < 2\sqrt{L/C}$).
- When SCR T is triggered, current flows from V_{dc} through T, L and the load and charges capacitor C. Because of resonance the current rises, reaches a peak and then **falls to zero naturally**.
- When the current falls below the holding current, **T turns OFF by itself**. The capacitor is now charged to nearly $2V_{dc}$ ($> V_{dc}$), so the SCR gets a reverse voltage for some time, which ensures

turn-off.

- The capacitor then discharges through the load and the circuit is ready for the next triggering.
- Used for high frequency (above 1 kHz) applications such as **series inverters**.

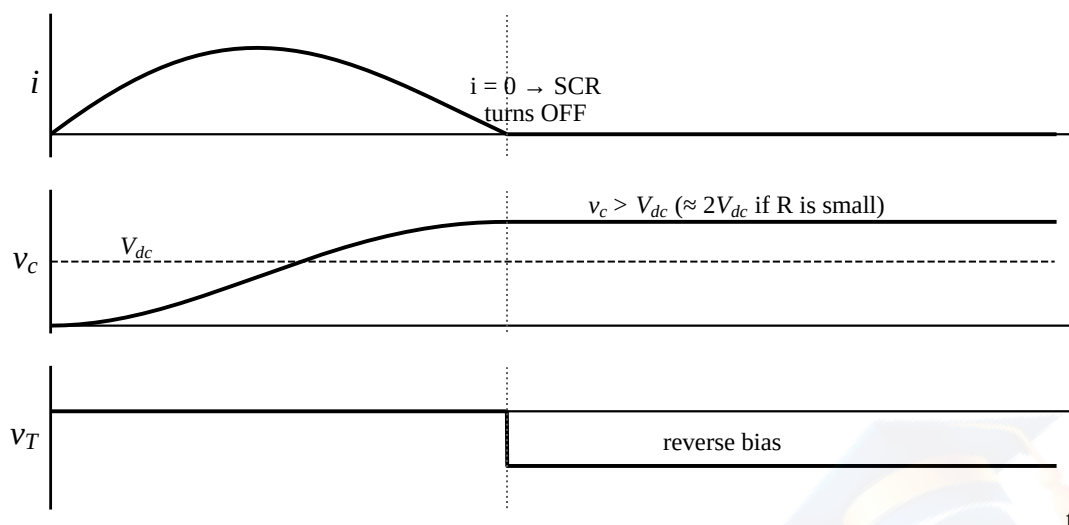


Fig.: Class A commutation — load current is oscillatory (computed for $\zeta = 0.15$)

(Circuit 1 M, waveforms 1 M, explanation 2 M)

d) 1- ϕ fully controlled bridge rectifier with R load ($\alpha = 60^\circ$, 230 V)

4 M

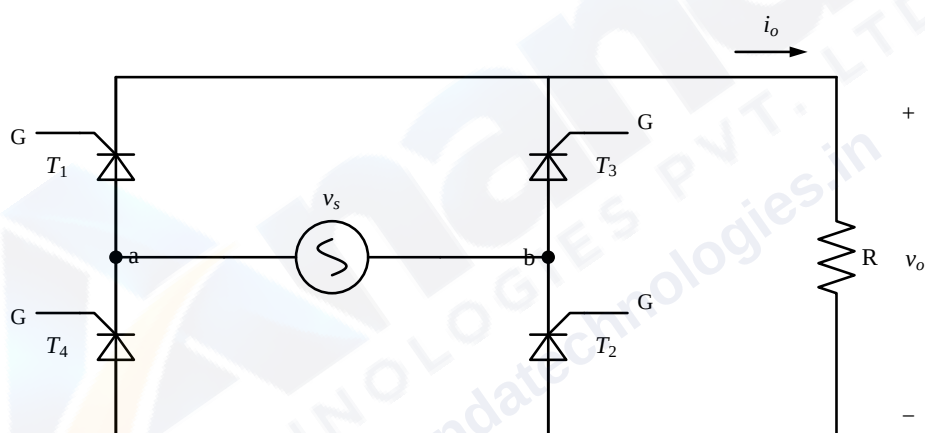


Fig.: Single phase fully controlled bridge rectifier with R load

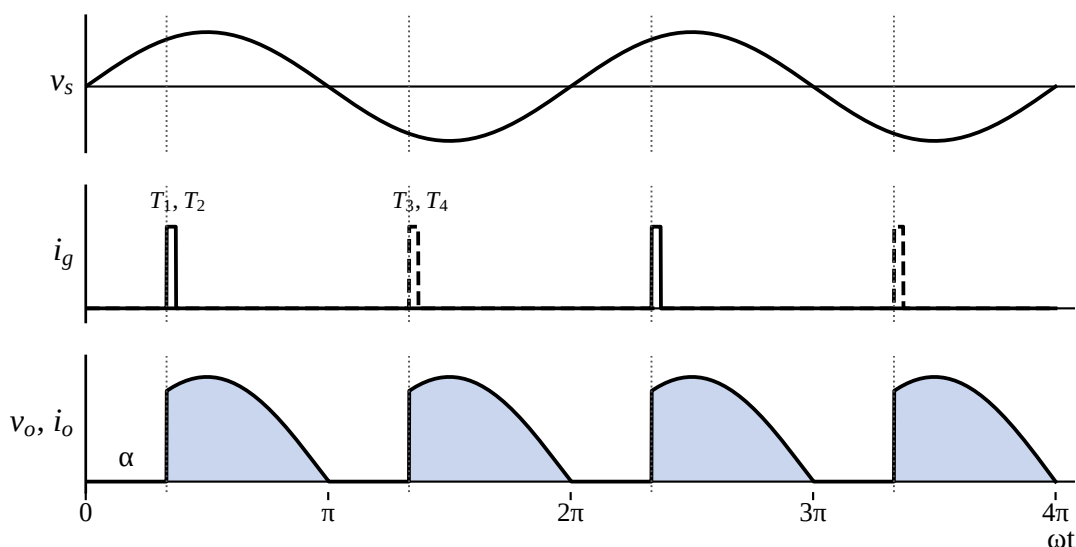


Fig.: Waveforms of 1- ϕ fully controlled bridge with R load ($\alpha = 60^\circ$)

- The bridge has four SCRs: T1, T2 conduct in the positive half cycle and T3, T4 in the negative half cycle.
- **Positive half cycle (0 to π):** a is positive w.r.t. b; T1 and T2 are forward biased. They are fired at $\omega t = \alpha$. Current flows $a \rightarrow T1 \rightarrow \text{load} \rightarrow T2 \rightarrow b$; $v_o = v_s$. At $\omega t = \pi$ current becomes zero and T1, T2 turn OFF (line commutation).
- **Negative half cycle (π to 2π):** b is positive; T3 and T4 are fired at $\omega t = \pi + \alpha$. Current flows $b \rightarrow T3 \rightarrow \text{load} \rightarrow T4 \rightarrow a$, in the **same direction** through the load; $v_o = -v_s$.
- Thus the output is a controlled full-wave DC voltage. Increasing α reduces the output.

Average output voltage: $V_{dc} = (V_m/\pi)(1 + \cos \alpha)$

$$V_m = \sqrt{2} \times 230 = 325.27 \text{ V}$$

$$V_{dc} = (325.27/\pi)(1 + \cos 60^\circ) = \mathbf{155.30 \text{ V}}$$

(Check: numerical average of the plotted waveform = 155.30 V)

(Circuit 1 M, waveform 1 M, working 1 M, calculation 1 M)

Q.3

a) dv/dt protection using snubber circuit

4 M

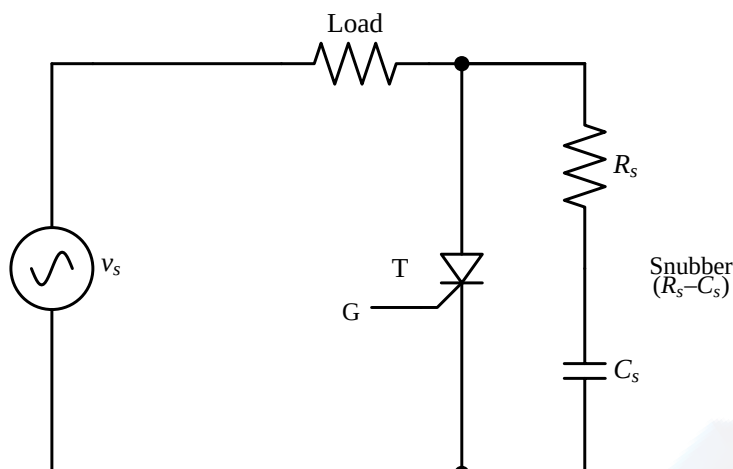


Fig.: RC snubber circuit for dv/dt protection of SCR

- When a forward voltage with very high rate of rise (dv/dt) appears across an SCR, the charging current of junction J2 capacitance ($i = C_j dv/dt$) may turn the SCR ON **falsely** (without gate signal).
- To prevent this an **RC snubber** (R_s in series with C_s) is connected **across (in parallel with) the SCR**.
- When the switch/supply voltage suddenly appears, C_s acts like a short circuit at the first instant and charges slowly; so the **voltage across the SCR rises slowly** and dv/dt is limited to a safe value.
- R_s limits the discharge current of C_s through the SCR when the SCR is turned ON (which would otherwise cause high di/dt) and damps oscillations.
- The snubber also suppresses voltage spikes during turn-off (reverse recovery) of the SCR.

(Circuit 2 M, explanation 2 M)

b) Need of freewheeling diode

4 M

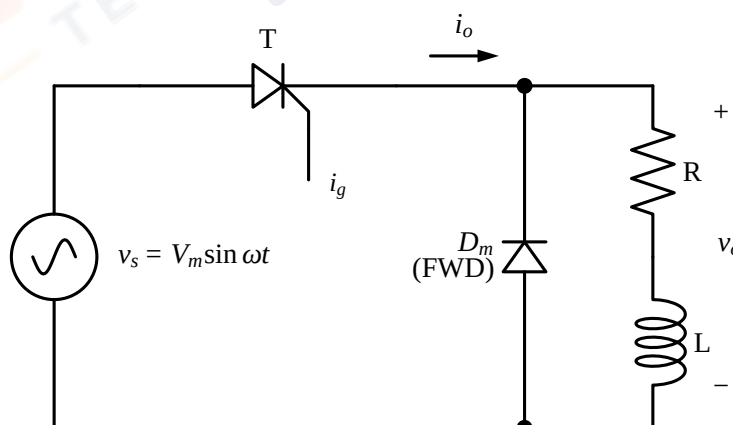


Fig.: Single phase half wave controlled rectifier with RL load and freewheeling diode

- **Prevents negative output voltage:** with R-L load, during the negative half cycle the FWD conducts and clamps v_o to zero, so the **average output voltage increases**.
- **Load current freewheels** through the diode; the load current becomes smoother / continuous.
- **SCR turns OFF at $\omega t = \pi$** (load current transfers to the FWD), so the SCR gets more time to turn off — commutation is improved.
- Energy stored in the inductance is dissipated in the load instead of being returned to the supply — **input power factor improves**.

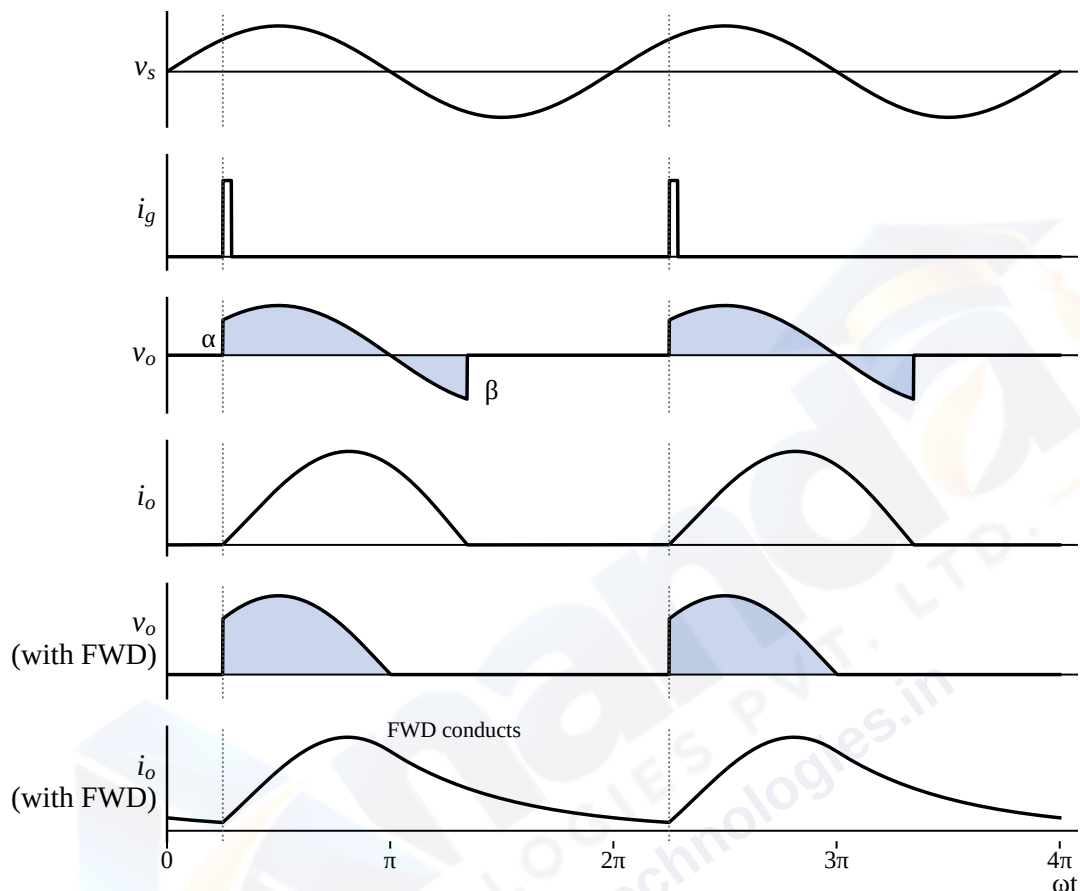


Fig.: Waveforms — R-L load ($\alpha = 45^\circ$); SCR conducts beyond π up to β because of L ; lower two: with freewheeling diode

Waveforms computed for $\alpha = 45^\circ$, load angle $\phi = \tan^{-1}(\omega L/R) = 60^\circ$: without FWD the SCR conducts up to $\beta = 242^\circ$, so v_o has a negative part; with FWD v_o is never negative.

(Need 2 M, diagram / waveform 2 M)

c) Need of PWM, types and single pulse modulation

4 M

Need of PWM in inverters:

- To **control the output voltage** of the inverter within the inverter itself (no extra controlled rectifier / chopper needed).
- To **reduce lower order harmonics** in the output; harmonics are shifted to higher frequency, so the filter becomes small and cheap.
- To get nearly **sinusoidal output** current for motors (less heating, noise and torque pulsation).
- To control voltage and frequency together (V/f control of induction motors).

Types of PWM: (1) Single pulse modulation, (2) Multiple pulse (uniform) modulation, (3) Sinusoidal pulse width modulation (SPWM), (4) Modified sinusoidal PWM (also phase-

displacement control).

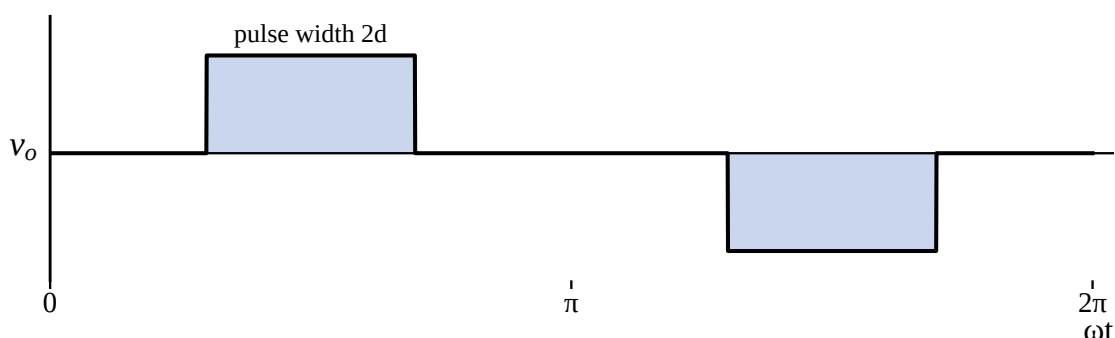


Fig.: Single pulse modulation — one pulse per half cycle, width controls output

Single pulse modulation: only **one pulse per half cycle** is produced, centred at $\pi/2$ (and $3\pi/2$). It is generated by comparing a rectangular reference with a triangular carrier; the pulse width $2d$ is varied (by changing the reference amplitude) to control the output voltage from zero to maximum. It has high lower-order harmonics (3rd, 5th) at low output.

(Need 1 M, types 1 M, single pulse with waveform 2 M)

d) R triggering circuit; why $\alpha \leq 90^\circ$

4 M

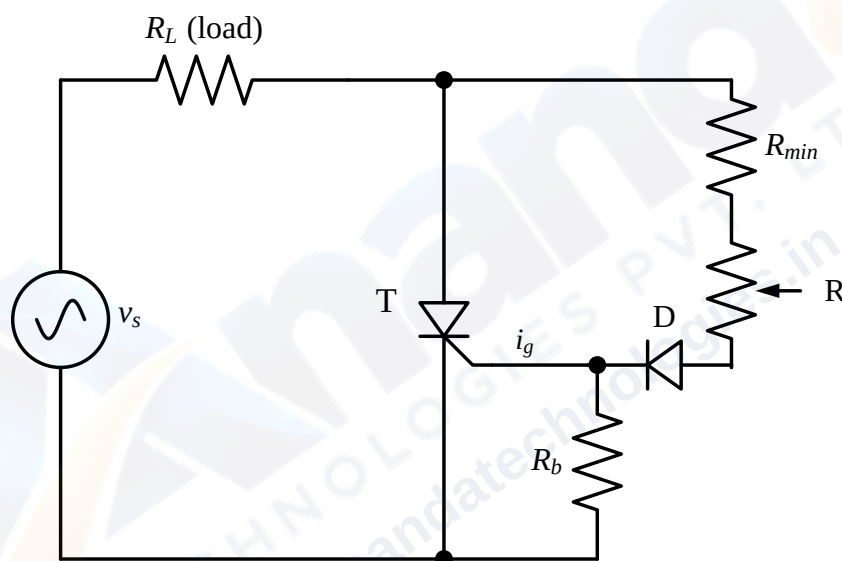


Fig.: Resistance (R) firing circuit of SCR

- R_{min} limits the peak gate current to a safe value when R is zero; R (variable) controls the gate current and hence the firing angle.
- Diode D allows gate current only in the positive half cycle and blocks reverse gate voltage in the negative half cycle.
- R_b limits the gate voltage (stabilising resistor) so that the gate voltage does not exceed its rating.
- In the positive half cycle the gate current rises with the supply voltage. The SCR fires when the gate voltage/current reaches the gate trigger value (V_{gt} , I_{gt}). Once ON, the voltage across the SCR falls to ≈ 1 V and the gate circuit current becomes almost zero.
- If R is increased, the gate current reaches I_{gt} later, so firing angle α increases and average load voltage decreases.

- **Limitation:** the gate current is maximum at $\omega t = 90^\circ$; hence α can be varied only from about 0° to 90° . If R is too large, the SCR does not fire at all.

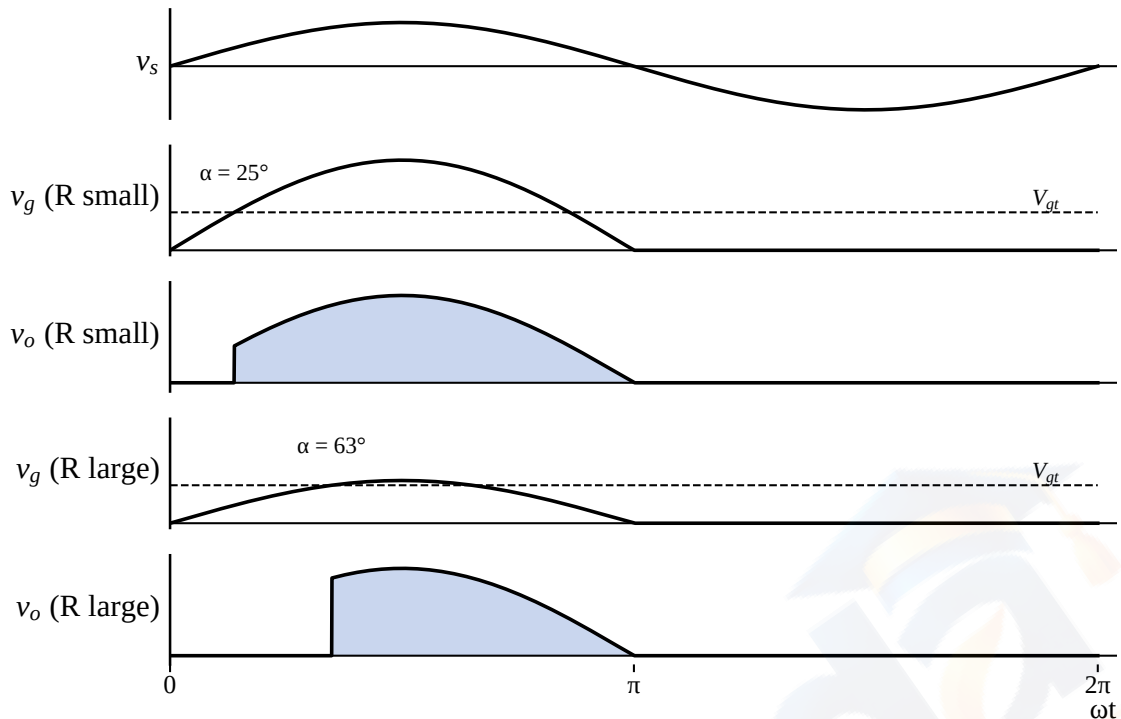


Fig.: Waveforms of R firing circuit — larger R gives larger α (maximum 90°)

Plotted example ($V_{gt} = 0.4$ of peak gate voltage): small $R \rightarrow \alpha \approx 25^\circ$, large $R \rightarrow \alpha \approx 63^\circ$.

Why α is limited to 90° : in R triggering the gate current is in phase with the supply voltage. It is maximum at $\omega t = 90^\circ$; if the gate current has not reached I_{gt} by 90° it decreases afterwards and the SCR never fires. Hence α can be varied only between 0° and 90° .

(Circuit 2 M, explanation 1 M, reason 1 M)

Q.4

a) 3- ϕ fully controlled bridge with R load, $\alpha = 30^\circ$

4 M

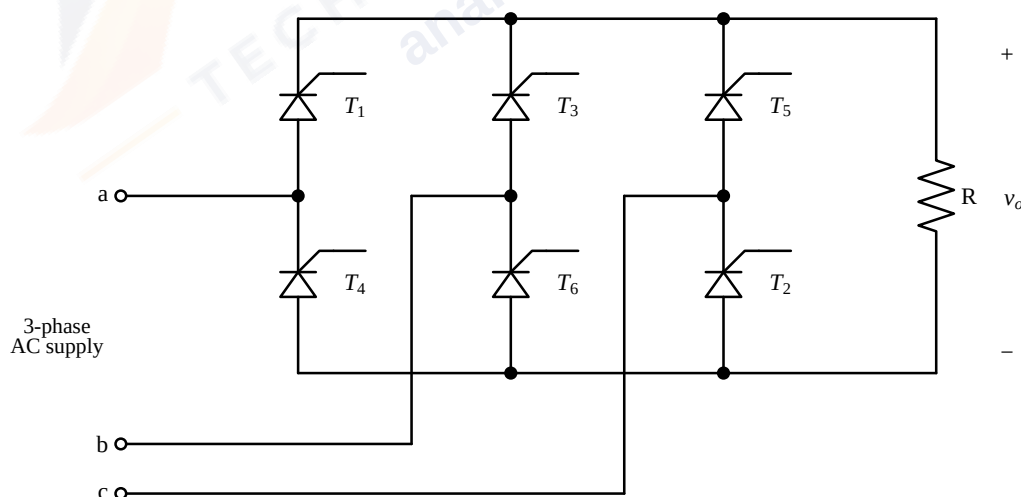


Fig.: Three phase fully controlled bridge rectifier with R load

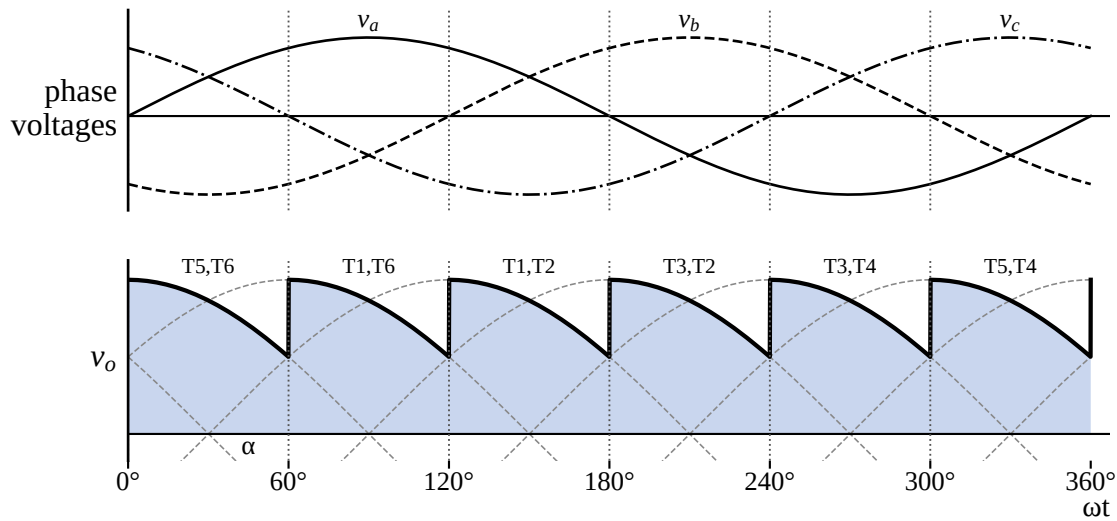


Fig.: Output voltage of 3- ϕ fully controlled bridge with R load ($\alpha = 30^\circ$); thin dashed curves are the six line voltages

- Six SCRs are used: **T1, T3, T5** form the positive (upper) group and **T4, T6, T2** the negative (lower) group. SCRs are numbered in the order of firing.
- At any time **two SCRs conduct** — one from the upper group connected to the most positive line and one from the lower group connected to the most negative line. The output is the corresponding line voltage.
- SCRs are fired at intervals of **60°** in the sequence T1 → T2 → T3 → T4 → T5 → T6; each SCR conducts for 120°. Conducting pairs: T6T1, T1T2, T2T3, T3T4, T4T5, T5T6.
- Firing angle α is measured from the **natural commutation point** (30° after the zero crossing of the phase voltage), i.e. the point where the diode in its place would start conducting.
- Output has **six pulses per cycle** (ripple frequency $6f = 300$ Hz), so ripple is small. With R load the output is continuous for $\alpha \leq 60^\circ$; for $\alpha > 60^\circ$ it becomes discontinuous.

Average output voltage: $V_{dc} = (3V_{ml}/\pi) \cos \alpha = 1.35 V_L \cos \alpha$ ($\alpha \leq 60^\circ$); $V_{dc} = (3V_{ml}/\pi)[1 + \cos(60^\circ + \alpha)]$ ($60^\circ \leq \alpha \leq 120^\circ$, R load)

$$V_L = 415 \text{ V}, V_{ml} = \sqrt{2} \times 415 = 586.90 \text{ V}, \alpha = 30^\circ$$

$$V_{dc} = \mathbf{485.36 \text{ V}} \text{ (numerical average of computed waveform = 485.36 V)}$$

(Circuit 2 M, waveform 2 M)

b) 1- ϕ half bridge inverter with R load

4 M

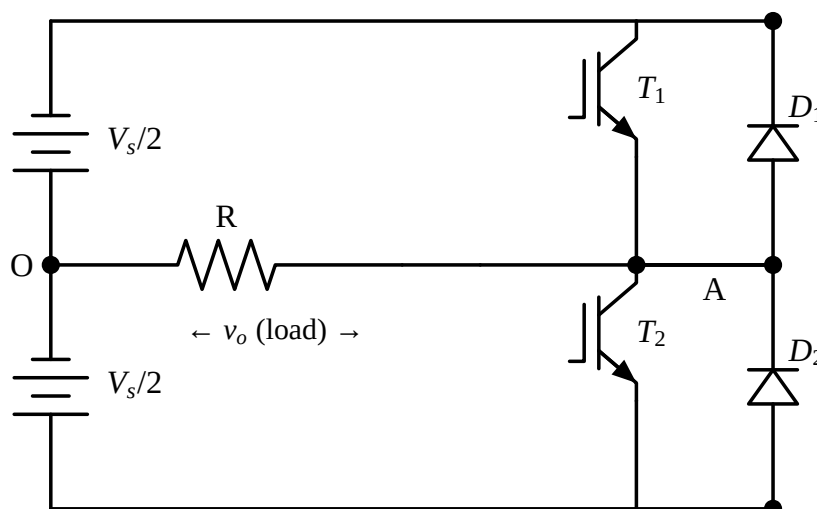


Fig.: Single phase half bridge inverter with R load

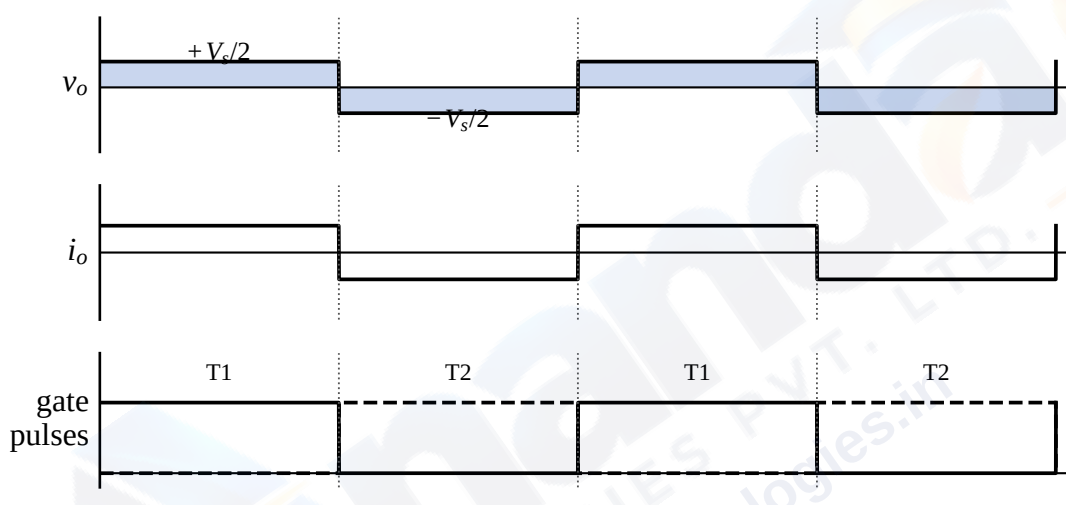


Fig.: Output waveforms of 1- ϕ half bridge inverter with R load

- The half bridge inverter uses **two switches T1, T2** (SCR/IGBT) and a **three-wire DC supply** (two equal sources $V_s/2$, or a centre-tapped capacitor divider). The load is connected between point A and the centre point O. D1, D2 are feedback diodes.
- $0 < t < T/2$: T1 is ON, T2 OFF. The upper source drives current from A to O through the load: $v_o = +V_s/2$.
- $T/2 < t < T$: T1 is turned OFF and T2 ON. The lower source drives current from O to A: $v_o = -V_s/2$.
- Thus a square wave AC of amplitude $V_s/2$ is obtained. Output frequency $f = 1/T$ is controlled by the rate of switching of T1 and T2. T1 and T2 must never be ON together (short circuit of supply).
- With R load the current is also a square wave in phase with voltage, so feedback diodes do not conduct; with R-L load they return reactive energy to the supply.

RMS output voltage $V_{o(rms)} = V_s/2$; RMS value of fundamental $V_{o1} = 2V_s/(\pi\sqrt{2}) = 0.45 V_s$.

(Circuit 1 M, waveforms 1 M, working 2 M)

c) Time ratio control strategies of chopper

4 M

In **time ratio control (TRC)** the average output $V_o = (T_{ON}/T)V_s$ is controlled by varying the ratio T_{ON}/T . Two methods are used:

- **(a) Constant frequency control (PWM):** chopping period T is kept constant and T_{ON} is varied (0 to T). Since frequency is fixed, the filter design is simple and harmonics are at known frequencies. It is the most commonly used method.
- **(b) Variable frequency control (FM):** T_{ON} is kept constant and T (frequency) is varied, or T_{OFF} is kept constant and T is varied. Filter design is difficult because frequency changes over a wide range; at low output current may become discontinuous.

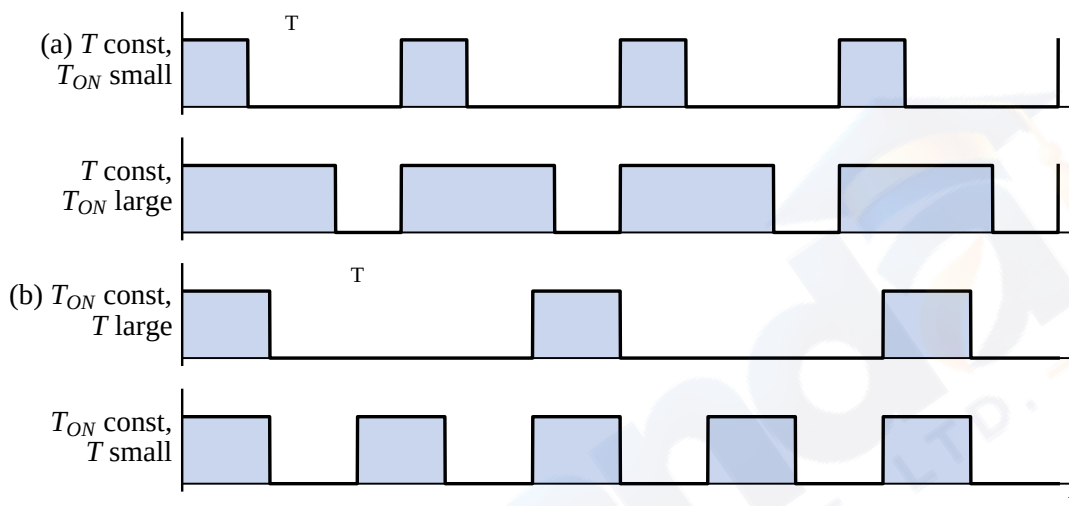


Fig.: Time ratio control — (a) constant frequency (PWM), (b) variable frequency

(Each method with waveform 2 M)

d) Speed control of ceiling fan using TRIAC

4 M

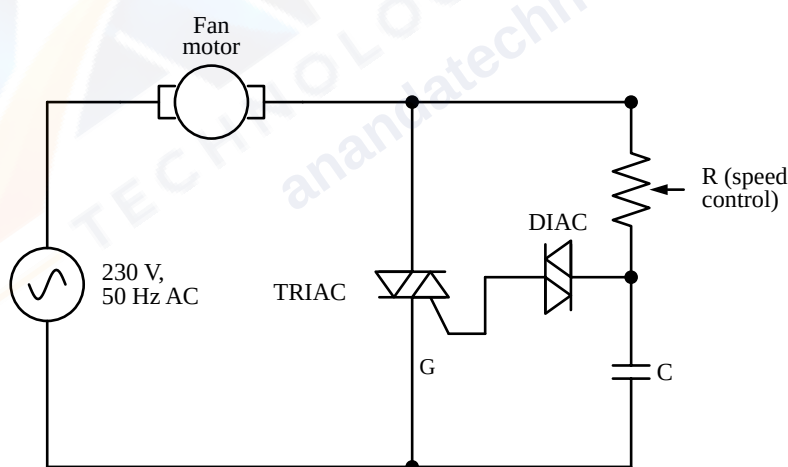


Fig.: Fan speed regulator using TRIAC and DIAC

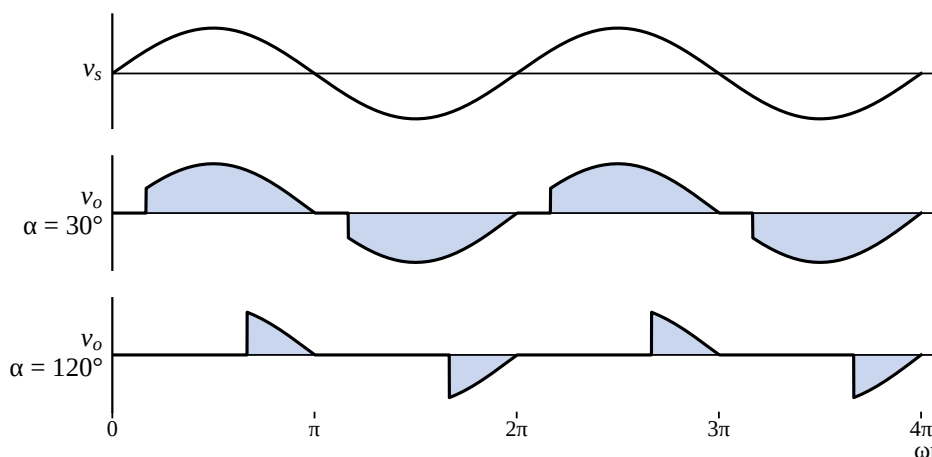


Fig.: Voltage across fan for two firing angles (small α = high speed, large α = low speed)

- The TRIAC is connected in series with the fan motor across the 230 V AC supply. An R-C network (R = speed control potentiometer) is connected across the TRIAC and a DIAC connects the R-C junction to the TRIAC gate.
- In each half cycle capacitor C charges through R. When the capacitor voltage reaches the **breakover voltage of the DIAC (≈ 30 V)**, the DIAC conducts and gives a gate pulse to the TRIAC.
- The TRIAC turns ON and applies the supply voltage to the fan for the rest of the half cycle; it turns OFF at current zero. Since TRIAC and DIAC are bidirectional, this happens in **both half cycles**.
- **Increasing R** $\rightarrow$ capacitor charges slowly $\rightarrow$ firing angle α increases $\rightarrow$ RMS voltage across fan decreases $\rightarrow$ **speed decreases**. Decreasing R increases speed. Thus smooth (stepless) speed control is obtained.

Advantages: very small power loss compared with resistive (rheostat) regulator, so electricity is saved; smooth stepless control; compact, light and cheap; long life (no moving contacts).

(Circuit 2 M, working 2 M)

e) AC to AC converter using DC link

4 M

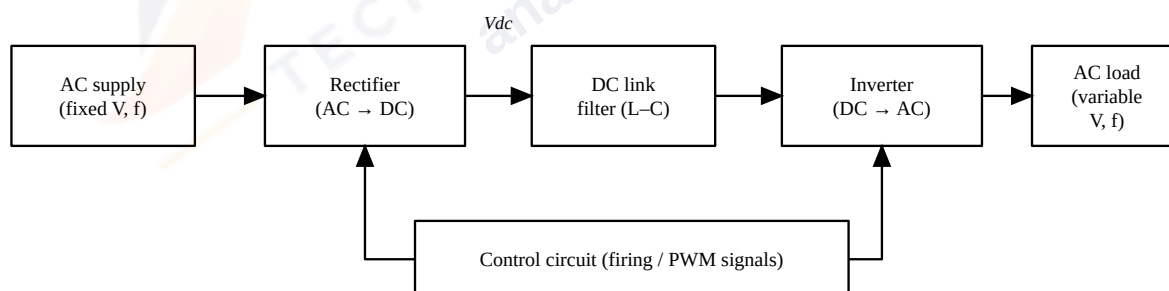


Fig.: Block diagram of AC to AC converter using DC link

- **Rectifier:** converts the fixed voltage, fixed frequency AC supply into DC (diode or SCR bridge).
- **DC link:** an L-C filter smooths the rectified voltage; the capacitor holds a steady DC voltage (V_{dc}) and decouples the two converters.

- **Inverter:** converts the DC link voltage into AC of the **required voltage and frequency** using PWM switching of IGBTs/MOSFETs.
- **Control circuit:** generates firing pulses for the rectifier and PWM pulses for the inverter according to the reference (speed / frequency).
- Thus AC of one frequency is converted to AC of another frequency in two stages (AC → DC → AC); output frequency is independent of input frequency.

(Block diagram 2 M, functions 2 M)

Q.5

a) V-I characteristics of SCR with effect of gate current

6 M

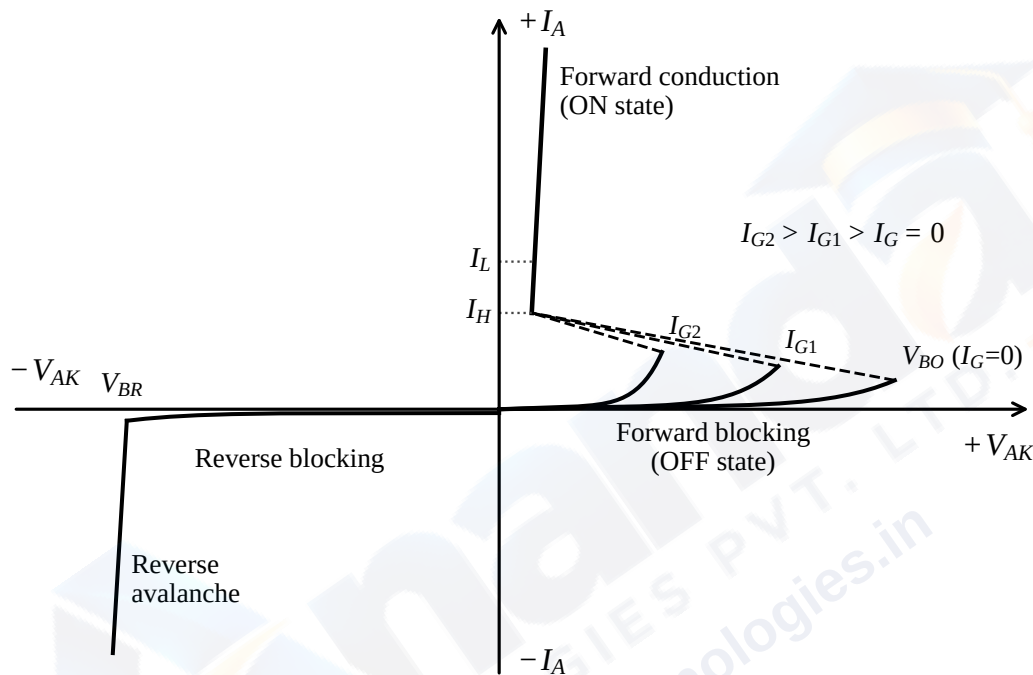


Fig.: V-I characteristics of SCR

- **Reverse blocking region:** Anode is negative w.r.t. cathode. Junctions J1 and J3 are reverse biased, so only a small reverse leakage current flows. If reverse voltage exceeds the reverse breakdown voltage V_{BR} , avalanche breakdown occurs and the SCR may be damaged.
- **Forward blocking (OFF) region:** Anode is positive w.r.t. cathode, gate open. J1 and J3 are forward biased but J2 is reverse biased, so only a small forward leakage current flows. The SCR is OFF.
- **Forward conduction (ON) region:** When the forward voltage reaches the forward breakover voltage V_{BO} , J2 breaks down and the SCR turns ON. The voltage across it falls to about 1–2 V and the current is limited only by the load.
- **Effect of gate current:** When gate current is applied, the SCR turns ON at a lower forward voltage. Larger gate current → smaller breakover voltage ($I_{G2} > I_{G1}$ gives lower V_{BO}).

Latching current (I_L): The minimum anode current that must flow through the SCR immediately after turn-ON (when the gate pulse is removed) to keep it latched in the ON state.

Holding current (I_H): The minimum anode current required to keep the SCR in the ON state. If the anode current falls below I_H , the SCR turns OFF. Normally $I_L \approx 2$ to 3 times I_H .

(Labelled characteristics 3 M, explanation of regions 2 M, I_L , I_H 1 M)

b) Step-down chopper; $V_s = 220$ V, $T_{ON} = 1.2$ ms, $T_{OFF} = 0.8$ ms

6 M

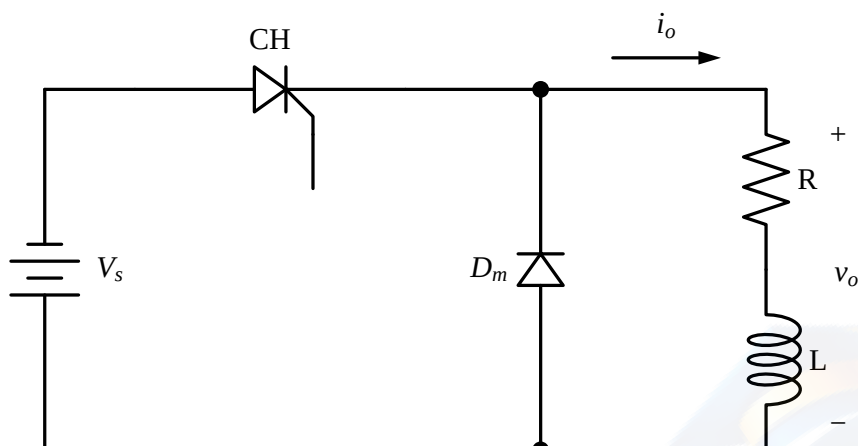


Fig.: Step-down (buck) chopper with RL load

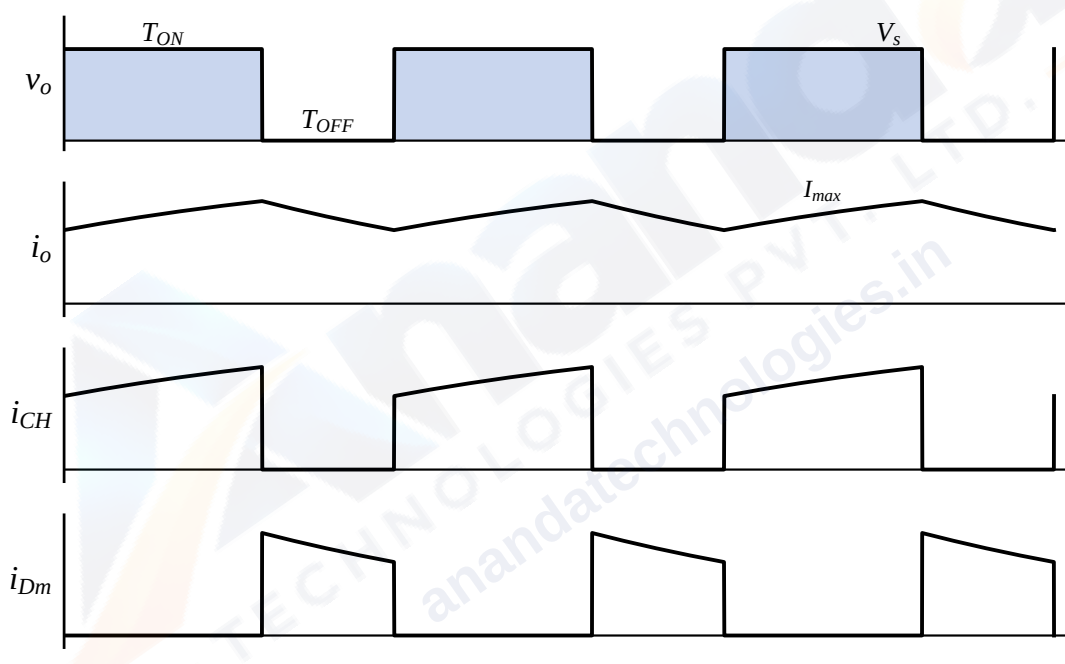


Fig.: Waveforms of step-down chopper ($D = 0.6$)

- A chopper CH (SCR with commutation circuit / MOSFET / IGBT) is connected in series with the load; D_m is the freewheeling diode.
- **T_{ON} period:** CH is ON, the supply is connected to the load; $v_o = V_s$. Load current rises exponentially and energy is stored in L. D_m is reverse biased.
- **T_{OFF} period:** CH is OFF; load current continues (freewheels) through D_m ; $v_o = 0$ and the current decays.
- The output is a chopped DC; its average value is less than V_s , hence **step-down (buck) chopper**. Output is controlled by varying duty cycle.

Output voltage: $V_o = (T_{ON} / (T_{ON} + T_{OFF})) \times V_s = (T_{ON}/T) V_s = D \cdot V_s$, where D = duty cycle ($0 \leq D \leq 1$)

Derivation: $v_o = V_s$ for $0 < t < T_{ON}$ and 0 for $T_{ON} < t < T$. Average $V_o = (1/T) \int_0^{T_{ON}} V_s dt = V_s T_{ON}/T = D \cdot V_s$.

$T = T_{ON} + T_{OFF} = 1.2 + 0.8 = 2.0$ ms; $D = 1.2/2.0 = 0.60$

$V_o = D \cdot V_s = 0.60 \times 220 = \mathbf{132.0\ V}$

Chopping frequency $f = 1/T = 1/(2 \times 10^{-3}) = \mathbf{500\ Hz}$

(Circuit 1 M, waveforms 1 M, working 2 M, equation 1 M, calculation 1 M)

c) 1- ϕ half controlled bridge with R-L load and FWD

6 M

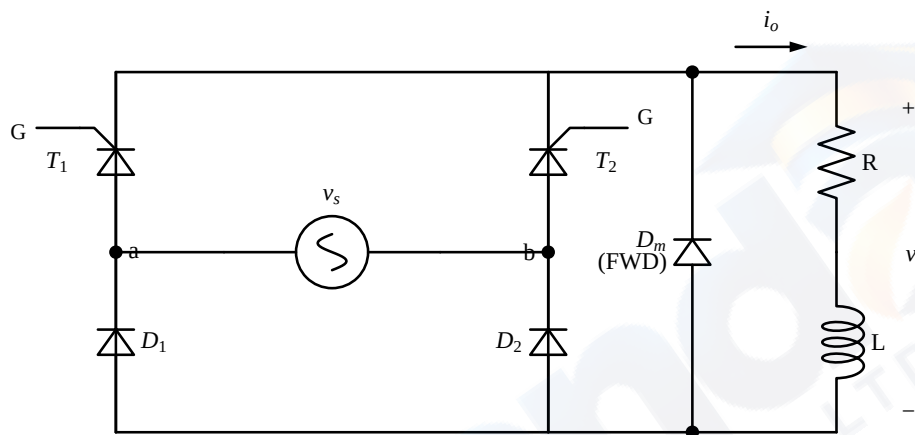


Fig.: Single phase half controlled (semi-converter) bridge rectifier with RL load and FWD

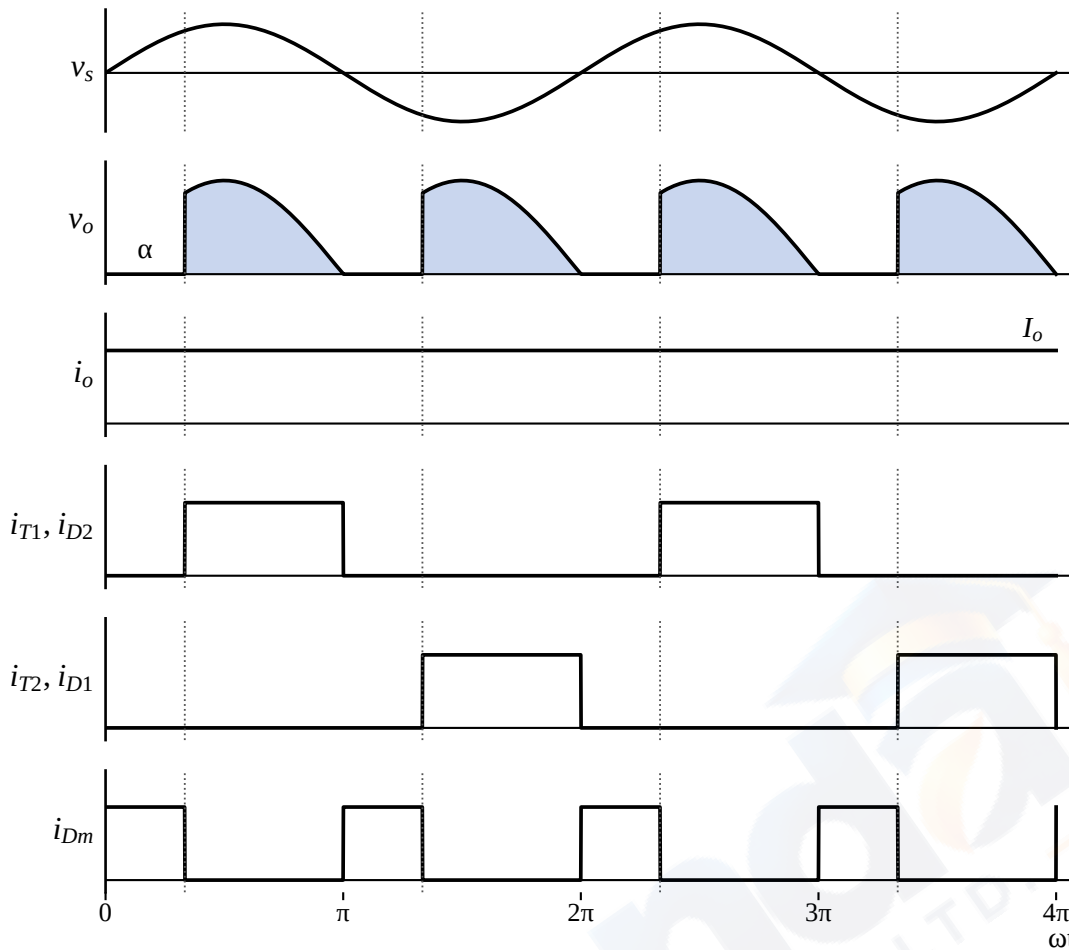


Fig.: Waveforms of 1-φ half controlled bridge with R-L load and FWD ($\alpha = 60^\circ$)

- The half controlled bridge (semi-converter) uses **two SCRs (T1, T2) and two diodes (D1, D2)**. D_m is the freewheeling diode across the highly inductive load (load current assumed continuous and ripple free, I_o).
- **α to π :** a is positive; T1 is fired at α . Current flows $a \rightarrow T1 \rightarrow \text{load} \rightarrow D2 \rightarrow b$; $v_o = v_s$.
- **π to $\pi + \alpha$:** supply reverses; v_o tends to become negative, so **D_m becomes forward biased** and the load current freewheels through it; $v_o = 0$. T1 is reverse biased and turns OFF (line commutation).
- **$\pi + \alpha$ to 2π :** T2 is fired; current flows $b \rightarrow T2 \rightarrow \text{load} \rightarrow D1 \rightarrow a$; $v_o = -v_s$ (positive).
- **2π to $2\pi + \alpha$:** D_m again freewheels. Thus the output voltage has **no negative part**; it is a one-quadrant converter.

Average output voltage: $V_{dc} = (V_m/\pi)(1 + \cos \alpha)$

(Circuit 2 M, waveforms 2 M, working 2 M)

Q.6

a) Construction and working of power MOSFET; characteristics

6 M

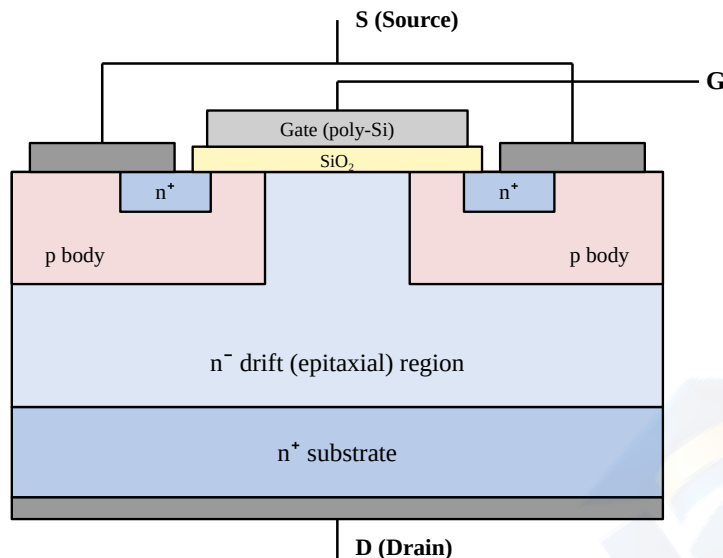


Fig.: Constructional details of n-channel enhancement power MOSFET

- Power MOSFET has a **vertical (DMOS) structure** so that current flows vertically from drain to source — large current and high voltage ratings are possible.
- The bottom **n⁺ substrate** forms the **Drain (D)**. Above it is a lightly doped **n⁻ drift (epitaxial) layer** which decides the blocking voltage.
- **p body** regions are diffused into the n⁻ layer and heavily doped **n⁺ source** regions are formed inside the p body.
- The **gate** (polysilicon) is placed over the p body between n⁺ source and n⁻ drift, insulated by a thin **SiO₂** layer.
- The **source metal** contacts both n⁺ source and p body (body–source short) to avoid turn-on of the parasitic BJT.

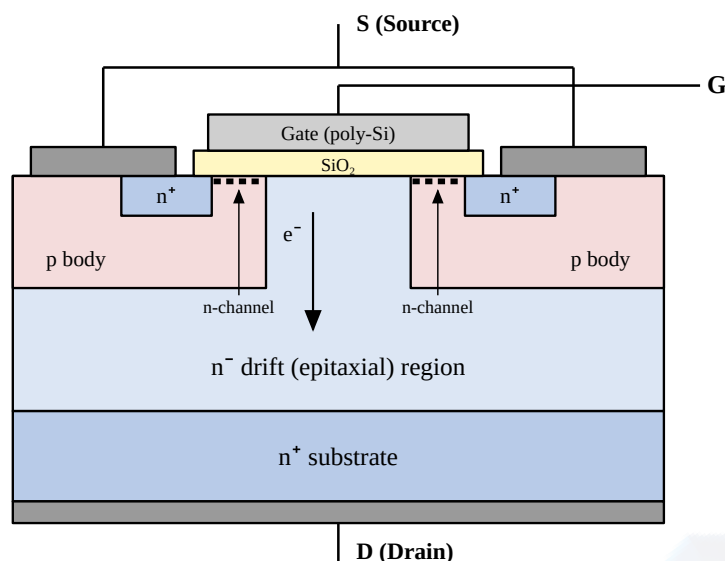


Fig.: n-channel E-type power MOSFET with positive gate voltage ($V_{GS} > V_{GS(th)}$)

- $V_{GS} = 0$: No channel; the p body – n^- drift junction is reverse biased, so no drain current flows. Device is OFF (enhancement type — normally OFF).
- V_{GS} positive ($> V_{GS(th)}$): Positive gate attracts electrons to the p-body surface below the gate. An **n-type inversion layer (channel)** is formed between n^+ source and n^- drift region.
- With V_{DS} positive, electrons flow from source $\rightarrow$ channel $\rightarrow$ drift region $\rightarrow$ drain; i.e. drain current I_D flows from drain to source.
- I_D increases with V_{GS} ; it is a **voltage controlled, majority carrier** device — very fast switching and almost zero gate current.
- Making V_{GS} zero removes the channel and the MOSFET turns OFF.

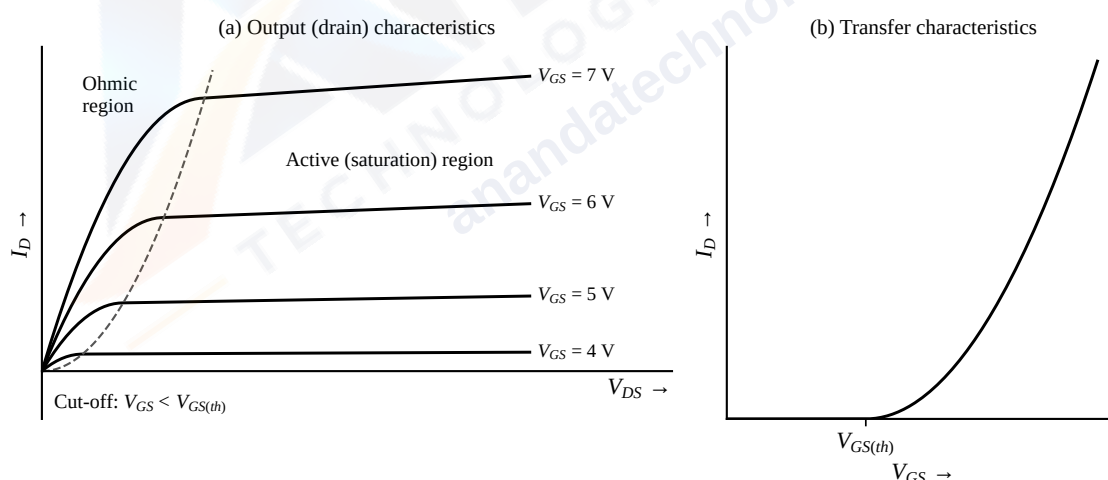


Fig.: Characteristics of n-channel enhancement power MOSFET

(Construction diagram 2 M, working 2 M, characteristics 2 M)

b) 1- ϕ full bridge inverter with R-L load; feedback diodes

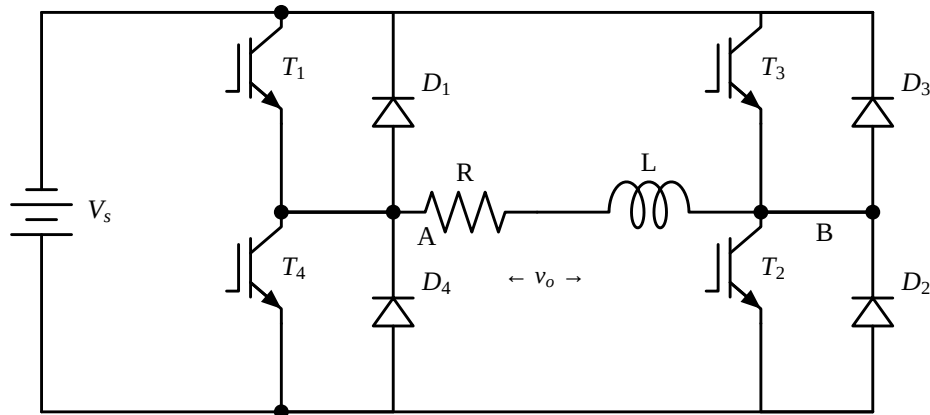


Fig.: Single phase full bridge inverter with RL load

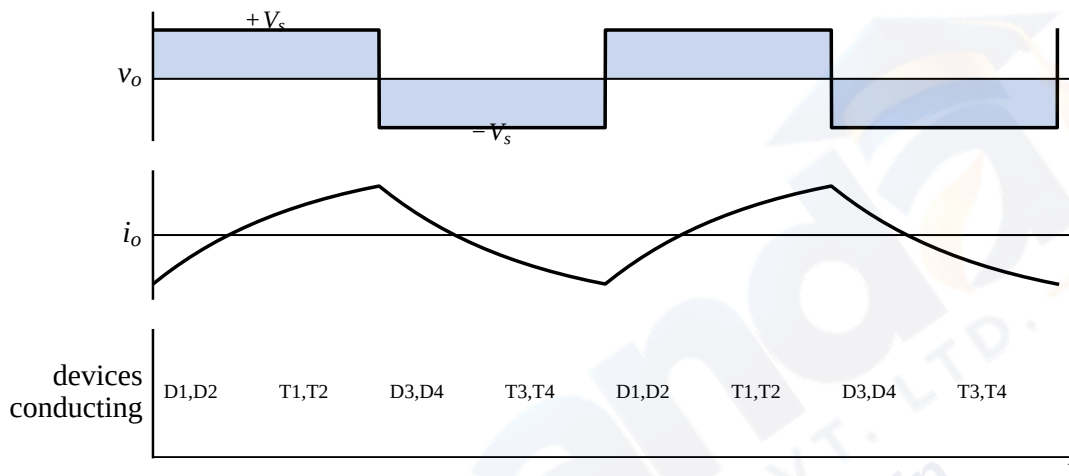


Fig.: Output waveforms of 1- ϕ full bridge inverter with RL load

- The full bridge inverter has **four switches T1–T4** with feedback diodes D1–D4 and a two-wire DC supply V_s . The load is connected between the leg mid-points A and B.
- $0 < t < T/2$: T1 and T2 are ON; A is connected to $+V_s$ and B to $-$; $v_o = +V_s$.
- $T/2 < t < T$: T1, T2 are turned OFF and T3, T4 ON; the load voltage reverses: $v_o = -V_s$.
- Output is a square wave of amplitude V_s (double that of half bridge for the same supply). Frequency is varied by changing the switching rate.
- With R-L load the current lags the voltage. When T1, T2 are turned OFF at $T/2$ the load current cannot reverse instantly; it continues in the same direction through **feedback diodes D3, D4**, returning stored energy to the source ($v_o = -V_s$).
- When the current reaches zero, T3, T4 (already gated) take over and the current builds up in the reverse direction. Similarly D1, D2 conduct at the start of the next positive half cycle.
- Load current is exponential (rising and falling) — conduction sequence per cycle: D1D2 $\rightarrow$ T1T2 $\rightarrow$ D3D4 $\rightarrow$ T3T4. (In the plotted case $\tau = L/R = 0.35T$, diodes conduct for 17 % of the period after each switching.)

RMS output voltage = V_s ; RMS value of fundamental $V_{o1} = 4V_s/(\pi\sqrt{2}) = 0.9 V_s$.

Function of feedback diodes: with inductive loads they provide a path for the load current after the switches are turned OFF, feed the reactive (stored) energy **back to the DC source**, and protect

the switches from high reverse / inductive voltage spikes.

(Circuit 2 M, waveforms 2 M, working 1 M, feedback diodes 1 M)

c) Solar PV system with charge controller; types

6 M

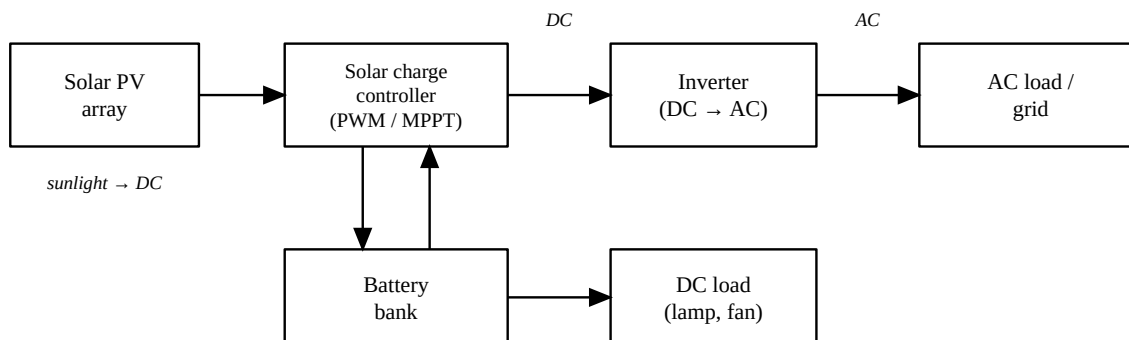


Fig.: Block diagram of solar PV power system with charge controller

- **Solar PV array:** series–parallel connected PV modules convert sunlight directly into DC electricity.
- **Solar charge controller:** regulates the voltage/current from the PV array to charge the battery safely; prevents **overcharging**, **deep discharge** and **reverse current** from battery to panel at night. Types: ON-OFF (series / shunt), PWM and MPPT.
- **Battery bank:** stores energy for use at night or on cloudy days.
- **Inverter:** converts DC into 230 V, 50 Hz AC for AC loads or grid connection. DC loads (LED lamps, DC fans) can be fed directly.

Types of solar charge controllers:

1. **ON-OFF (series / shunt) controller** — simple relay/switch type; disconnects panel when battery is full.
2. **PWM charge controller** — switches the panel to battery connection at high frequency; reduces charging current gradually as the battery fills.
3. **MPPT charge controller** — uses a DC-DC converter to operate the PV array at its **maximum power point**; 20–30 % more energy; used in larger systems.

(Block diagram 2 M, explanation 2 M, types 2 M)

Note: This is a **model question paper prepared by Ananda Technologies** only for practice and exam preparation, based on the pattern of previous MSBTE question papers and the K-scheme syllabus. It is **not an official MSBTE paper**, and it does **not** mean that these questions will come in the exam. Answers follow standard textbook points; marks shown are indicative. Free for students — anandatechnologies.in