Digital Techniques (313303)

MSBTE Diploma · K-Scheme · Model Question Paper — Set A

Time: 3 Hours **Max. Marks: 70**

Instructions:

1. All questions are compulsory.
2. Answer each next main question on a new page.
3. Illustrate your answers with neat sketches wherever necessary.
4. Figures to the right indicate full marks.
5. Assume suitable data, if necessary.
6. Use of non-programmable electronic pocket calculator is permissible.
7. Mobile phone, pager and any other electronic communication devices are not permissible in the examination hall.

Q.1 Attempt any FIVE of the following: **10**

a) State the base (radix) and the symbols used in binary, octal, decimal and hexadecimal number systems.

b) Draw the logic symbol and write the truth table of EX-OR gate.

c) State the commutative and associative laws of Boolean algebra.

d) Write the excitation table of J-K flip-flop.

e) List any four applications of multiplexer.

f) Define modulus of a counter. How many flip-flops are required to build a MOD-12 counter?

g) State any two differences between SRAM and DRAM.

Q.2 Attempt any THREE of the following: **12**

a) Convert the following:
i) $(157.625)_{10} = (?)_2$ ii) $(3B9)_{16} = (?)_8$ iii) $(725)_{10} = (?)_{BCD}$ iv) $(110101)_2 = (?)_{Gray}$

b) Realize NOT, AND, OR and NOR gates using only NAND gates.

c) Design a half adder. Write its truth table, simplify the outputs using K-map and draw the logic diagram.

d) Describe the working of clocked J-K flip-flop with logic diagram (using NAND gates) and truth table.

Q.3 Attempt any THREE of the following: **12**

a) Minimize the following expression using K-map and draw the logic diagram:
$F(A, B, C, D) = \Sigma m\ (1, 3, 4, 5, 9, 11, 12, 13)$

b) Perform the subtraction $(46)_{10} - (75)_{10}$ using 2's complement method.

c) Design a 16 : 1 multiplexer using 4 : 1 multiplexers.

d) Draw the circuit diagram of 4-bit weighted resistor DAC and derive the expression for its output voltage.

Q.4 Attempt any THREE of the following: **12**

a) State and prove De Morgan's theorems. Draw the logic diagram for each theorem.

b) Draw and explain a 4-bit SISO shift register using D flip-flops. Show the shifting of serial data 1010 with a table and waveforms.

c) Compare TTL and CMOS logic families on the basis of: i) propagation delay ii) power dissipation iii) noise margin iv) fan-out.

d) Draw the block diagram of BCD to 7-segment decoder (common cathode display) and write its truth table.

e) What is race-around condition in J-K flip-flop? How is it avoided in master-slave J-K flip-flop?

Q.5 Attempt any TWO of the following: **12**

a) Define SOP and POS forms. Convert F(A, B, C) = Σm (0, 2, 3, 6, 7) into standard POS form. Also minimize F using K-map and draw the logic diagram.

b) Design a MOD-10 asynchronous (ripple) counter using J-K flip-flops. Write its truth table and draw the timing diagram.

c) Draw a 4-bit R-2R ladder DAC and explain its working. Calculate the output voltage for digital input 1010 if $V_R = 5$ V and $R_f = R$.

Q.6 Attempt any TWO of the following: **12**

a) Design a 3-bit synchronous up counter using J-K flip-flops. Show the excitation table, K-maps, logic diagram and output waveforms.

b) Compare the following (any three points each): i) Volatile and non-volatile memory ii) EPROM and EEPROM.

c) Draw the block diagram of successive approximation type ADC and explain its working with a 4-bit example. Give two applications of ADC.

Note: This is a **model question paper prepared by Ananda Technologies** only for practice and exam preparation, based on the pattern of previous MSBTE question papers and the K-scheme syllabus. It is **not an official MSBTE paper**, and it does **not** mean that these questions will come in the exam. Answers follow standard textbook points; marks shown are indicative. Free for students — anandatechnologies.in