

Digital Techniques (313303)

MSBTE Diploma · K-Scheme · Model Question Paper — Set B

Time: 3 Hours**Max. Marks: 70****Instructions:**

1. All questions are compulsory.
2. Answer each next main question on a new page.
3. Illustrate your answers with neat sketches wherever necessary.
4. Figures to the right indicate full marks.
5. Assume suitable data, if necessary.
6. Use of non-programmable electronic pocket calculator is permissible.
7. Mobile phone, pager and any other electronic communication devices are not permissible in the examination hall.

Q.1 Attempt any FIVE of the following:**10**

- a) Convert $(93)_{10}$ into hexadecimal and octal numbers.
- b) State the duality theorem and give one example.
- c) Draw the logic symbol and write the truth table of NOR gate.
- d) State the function of encoder and decoder. Give one application of each.
- e) Write the excitation tables of T flip-flop and D flip-flop.
- f) List the modes of operation of shift register.
- g) State De Morgan's theorems and write their logical expressions.

Q.2 Attempt any THREE of the following:**12**

- a) Convert $(11010110)_2$ into decimal, hexadecimal, Gray code and Excess-3 code.
- b) Realize OR, AND, NOT and NAND gates using only NOR gates. Write the expression at each stage.
- c) Design a full adder using K-map and draw its logic diagram.
- d) Draw and explain a 4-bit ring counter using D flip-flops with its truth table and waveforms.

Q.3 Attempt any THREE of the following:**12**

- a) Minimize the following expression using K-map and draw the logic diagram:
 $F(A, B, C, D) = \Pi M(0, 1, 4, 5, 6, 10, 11, 14, 15)$
- b) Perform BCD addition: i) $(2759)_{10} + (4386)_{10}$ ii) $(68)_{10} + (57)_{10}$
- c) Design a 16 : 1 multiplexer using 8 : 1 multiplexers and a 2 : 1 multiplexer. Explain how input I_{12} is selected.
- d) Draw a clocked S-R flip-flop using NAND gates and explain its working with truth table.

Q.4 Attempt any THREE of the following:

12

- Simplify the following expression using Boolean laws (write the law used in each step) and draw the logic diagram:

$$Y = \overline{A}BC + \overline{A}BC + \overline{A}BC + ABC + ABC$$
- Draw and explain 4 : 2 priority encoder with block diagram, truth table and logic diagram.
- A 4-bit R-2R ladder DAC has $V_R = 10\text{ V}$ and $R_f = R$. Calculate the output voltage for digital inputs i) 1101 ii) 0110. Also find its resolution.
- Compare SRAM and DRAM. (Any four points)
- Explain buffer and tri-state buffer with logic symbol and truth table. Give one application of each.

Q.5 Attempt any TWO of the following:

12

- Explain BCD to 7-segment decoder with truth table and block diagram. Simplify the logic for segments 'c' and 'f' using K-map and draw their logic diagrams.
- Describe the working of master-slave J-K flip-flop with logic diagram, truth table and timing diagram.
- Design a MOD-6 synchronous counter using J-K flip-flops. Draw the logic diagram and timing diagram.

Q.6 Attempt any TWO of the following:

12

- Explain 1 : 4 demultiplexer with truth table and logic diagram. Design a 1 : 16 demultiplexer using 1 : 4 demultiplexers.
- Draw the block diagram of dual slope ADC and explain its working with waveforms. State any two specifications of ADC.
- Convert the following:
 i) $(B4E.6)_{16} = (?)_{10}$ ii) $(247.3)_{10} = (?)_8$ iii) $(0110\ 1001\ 0111)_{BCD} = (?)_2$

Note: This is a **model question paper prepared by Ananda Technologies** only for practice and exam preparation, based on the pattern of previous MSBTE question papers and the K-scheme syllabus. It is **not an official MSBTE paper**, and it does **not** mean that these questions will come in the exam. Answers follow standard textbook points; marks shown are indicative. Free for students — anandatechnologies.in