

Fundamentals of Power Electronics (313335)

MSBTE K-Scheme · EE Sem III · Model Question Paper — Set C · Model Answers

Answers are written point-wise as expected in MSBTE model answers. Marks scheme lines in blue italics are indicative. All waveforms are plotted from the circuit equations and all numerical values were calculated by program.

Q.1

a) Applications of power electronics

2 M

1. Speed control of DC and AC motors (drives, traction, fans, pumps, rolling mills)
2. Controlled rectifiers, battery chargers, electroplating and welding power supplies
3. Inverters, UPS and SMPS for computers and telecom
4. Renewable energy: solar inverters, MPPT charge controllers, wind power converters

(Any four, ½ M each)

b) Symbols of SCR, TRIAC and power MOSFET

2 M

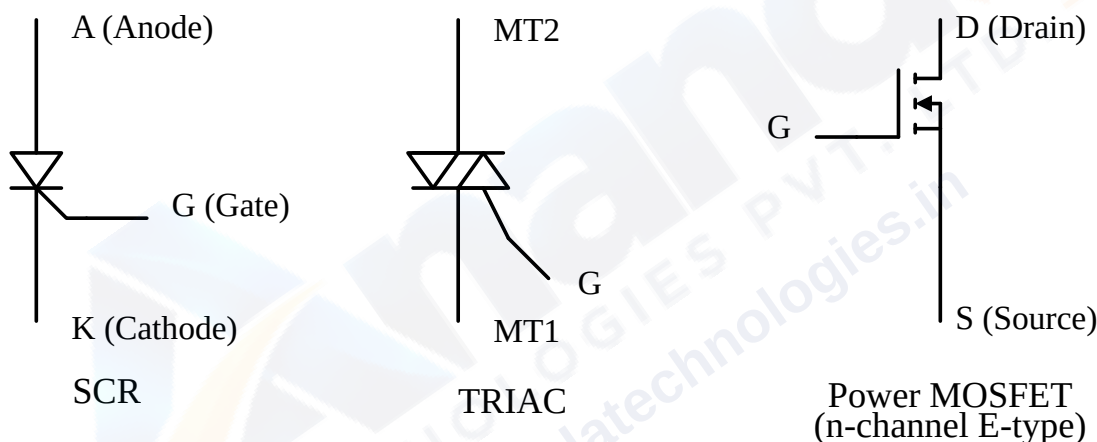


Fig.: Symbols of SCR, TRIAC and power MOSFET

(Symbols with terminals)

c) Triggering; turn-ON methods

2 M

Triggering: The process of turning ON an SCR (bringing it from the forward blocking state to the forward conducting state) is called triggering.

1. **Forward voltage triggering** — V_{AK} increased above breakover voltage V_{BO}
2. **Gate triggering** — positive gate current applied (most common and reliable method)
3. **dv/dt triggering** — fast rising anode voltage; charging current of junction capacitance turns it ON
4. **Thermal (temperature) triggering** — high junction temperature increases leakage current

(Definition 1 M, methods 1 M)

d) Chopping period, duty cycle; V_o for 200 V, $D = 0.4$

2 M

- **Chopping period (T):** the total time of one ON–OFF cycle, $T = T_{ON} + T_{OFF}$. Chopping frequency $f = 1/T$.
- **Duty cycle (D or α):** the ratio of ON time to chopping period, $D = T_{ON}/T = T_{ON}/(T_{ON} + T_{OFF})$; $0 \leq D \leq 1$.

$$V_o = D \times V_s = 0.4 \times 200 = \mathbf{80 \text{ V}}$$

(Definitions 1 M, calculation 1 M)

e) Controlled vs uncontrolled rectifier

2 M

Controlled rectifier	Uncontrolled rectifier
Uses SCRs (thyristors)	Uses diodes
Output DC voltage can be varied by changing firing angle α	Output DC voltage is fixed
Needs gate (firing) circuit	No gate / control circuit
Costlier; used in DC drives, battery chargers	Cheaper; used in fixed DC supplies

(Any two points, 1 M each)

f) Photovoltaic cell

2 M

Photovoltaic (PV) cell: A PV (solar) cell is a semiconductor p-n junction device (usually silicon) which converts **light (solar) energy directly into electrical (DC) energy** by the photovoltaic effect. One silicon cell gives about 0.5–0.6 V; cells are connected in series/parallel to form modules and arrays.

(Definition 2 M)

g) Methods of SCR protection

2 M

1. Over-voltage protection — RC snubber, MOV / selenium suppressor, crowbar
2. Over-current protection — fast acting fuse, circuit breaker, current limiting reactor
3. dv/dt protection — RC snubber across SCR
4. di/dt protection — inductor in series with SCR
5. Gate protection and thermal protection (heat sink)

(Any four, $\frac{1}{2}$ M each)

Q.2

a) Construction of IGBT; advantages

4 M

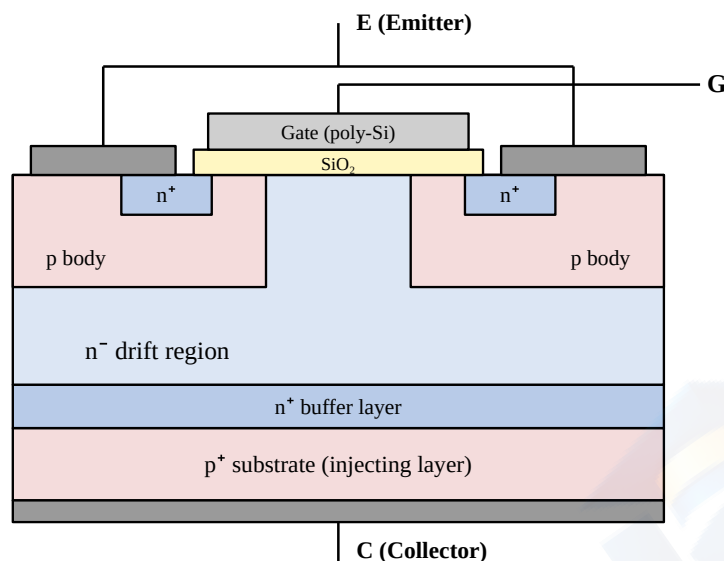


Fig.: Constructional details of IGBT

- IGBT is a **four-layer ($p^+ n^+ n^- p n^+$)** device with three terminals: **Collector (C)**, **Gate (G)** and **Emitter (E)**.
- Its construction is similar to a vertical power MOSFET, except that the n^+ drain substrate is replaced by a **p^+ substrate** called the **injecting layer**; the collector metal is attached to it.
- Above the p^+ layer is an **n^+ buffer layer** (in punch-through IGBT) and a lightly doped **n^- drift region** which blocks the forward voltage.
- **p body** regions are diffused into the drift region and **n^+ emitter** regions are diffused into the p body. The emitter metal touches both n^+ and p body (short).
- The **gate** (polysilicon) is insulated from the p body by a thin **SiO_2** layer, so the gate draws almost no current (high input impedance, like MOSFET).

Advantages of IGBT: (i) voltage controlled — simple gate drive, negligible gate current (like MOSFET); (ii) low ON-state voltage drop and high current capability due to conductivity modulation (like BJT); (iii) fast switching (up to ~20–50 kHz) and no secondary breakdown.

(Diagram 2 M, description 1 M, advantages 1 M)

b) Light triggering of SCR

4 M

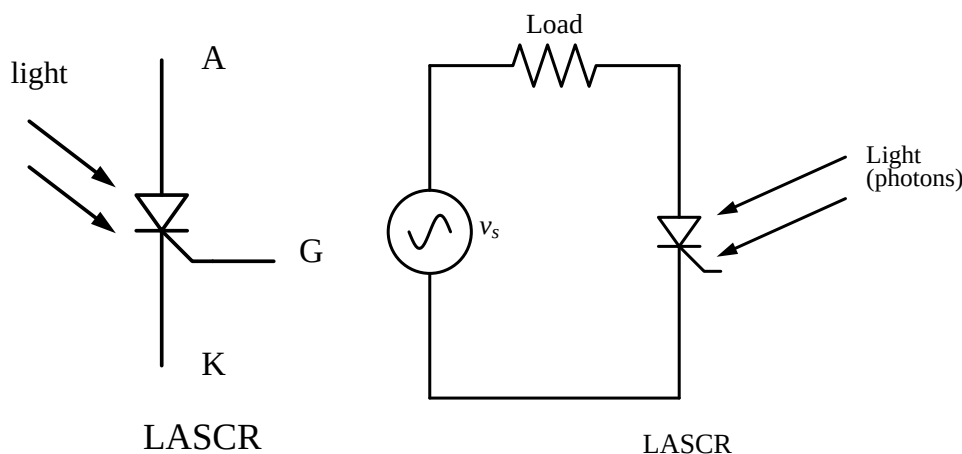


Fig.: Symbol of LASCR

Fig.: Light triggering of LASCR

- In light triggering a special SCR called **LASCR (Light Activated SCR)** is used. A small window/niche is provided in the inner P layer (gate region) near junction J2.
- When light (photons) of sufficient intensity falls on the junction, **electron-hole pairs are generated**; this increases the leakage current through J2.
- When the current reaches the latching level, regenerative action starts and the **SCR turns ON** without any electrical gate connection.
- Light can be sent through **optical fibre**, giving complete **electrical isolation** between the high-voltage power circuit and the low-voltage control circuit.
- **Applications:** HVDC transmission (series strings of SCRs), static VAR compensators, opto-couplers and optical relays.

(Symbol/diagram 1 M, explanation 3 M)

c) Self (class A) commutation; why "load commutation"

4 M

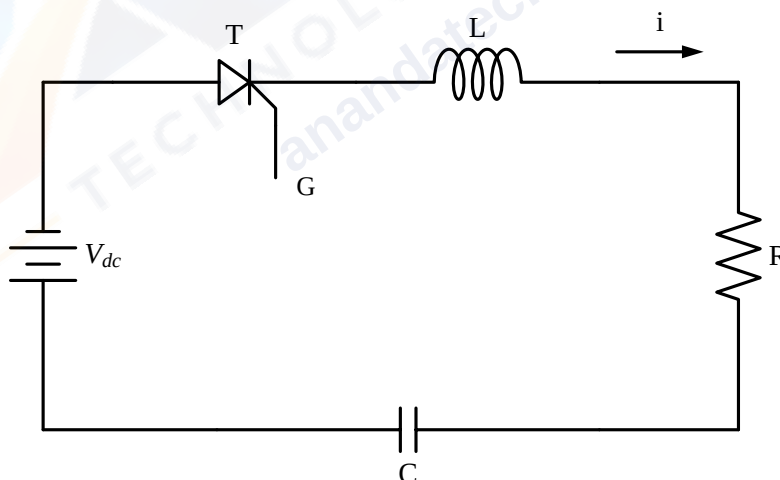


Fig.: Class A (resonant / load) commutation circuit

- Class A is also called **self commutation, load commutation or resonant commutation**.
- An inductor L and capacitor C are connected with the load so that the circuit is **under-damped** (for series R-L-C: $R < 2\sqrt{L/C}$).

- When SCR T is triggered, current flows from V_{dc} through T, L and the load and charges capacitor C. Because of resonance the current rises, reaches a peak and then **falls to zero naturally**.
- When the current falls below the holding current, **T turns OFF by itself**. The capacitor is now charged to nearly $2V_{dc}$ ($> V_{dc}$), so the SCR gets a reverse voltage for some time, which ensures turn-off.
- The capacitor then discharges through the load and the circuit is ready for the next triggering.
- Used for high frequency (above 1 kHz) applications such as **series inverters**.

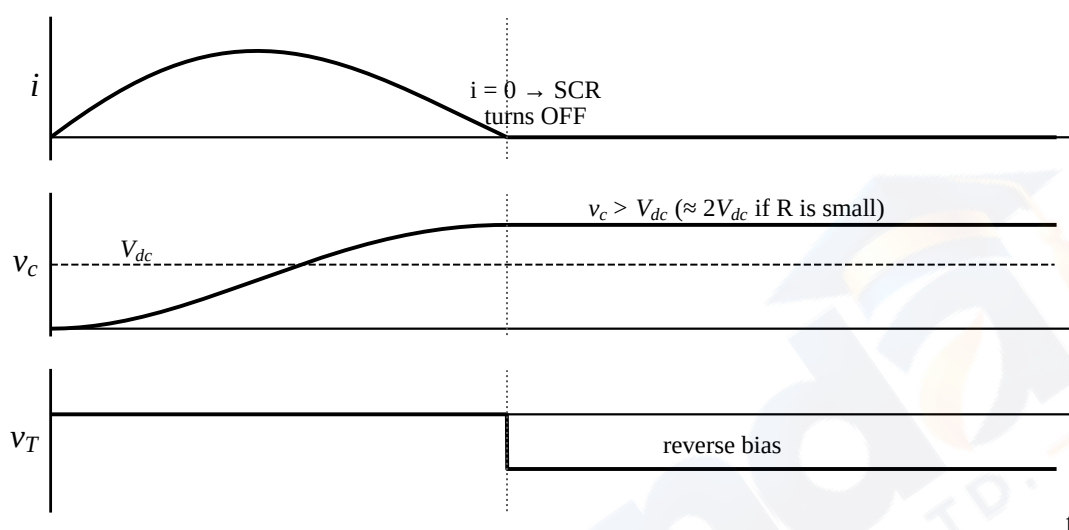


Fig.: Class A commutation — load current is oscillatory (computed for $\zeta = 0.15$)

Why called load commutation: the commutating elements L and C are connected **in series / parallel with the load** and the load current itself becomes zero by resonance; the SCR is turned off by the behaviour of the load circuit, without any auxiliary SCR or external pulse.

(Circuit 1 M, waveform 1 M, explanation 1 M, reason 1 M)

d) 1- ϕ fully controlled bridge, R load: 230 V, $R = 20 \Omega$, $\alpha = 45^\circ$

4 M

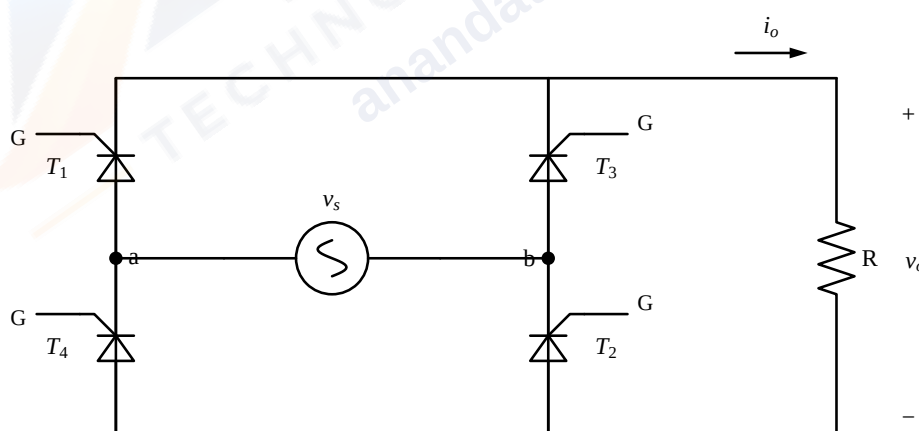


Fig.: Single phase fully controlled bridge rectifier with R load

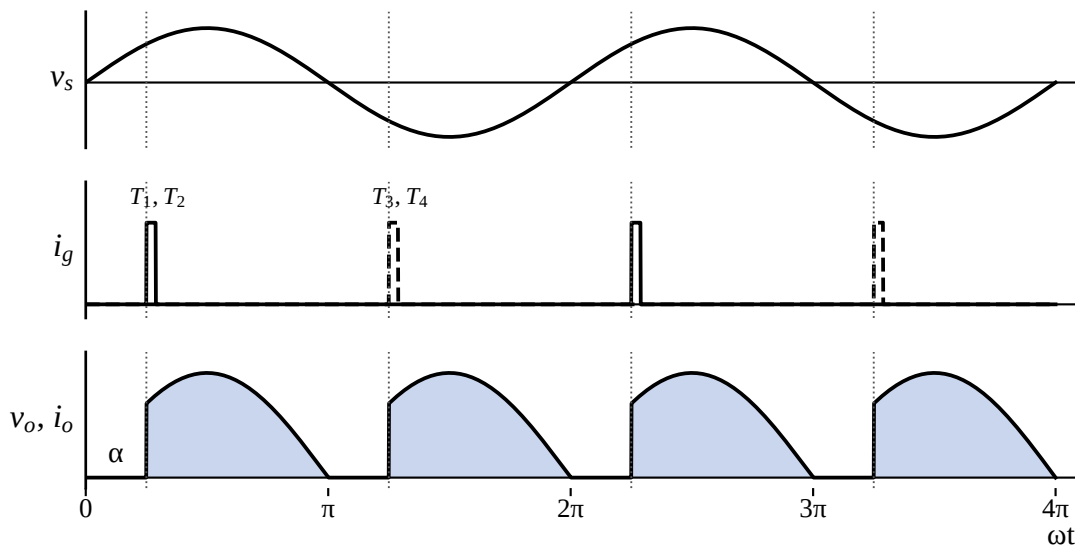


Fig.: Waveforms of 1-φ fully controlled bridge with R load ($\alpha = 45^\circ$)

- The bridge has four SCRs: T1, T2 conduct in the positive half cycle and T3, T4 in the negative half cycle.
- **Positive half cycle (0 to π):** a is positive w.r.t. b; T1 and T2 are forward biased. They are fired at $\omega t = \alpha$. Current flows $a \rightarrow T1 \rightarrow \text{load} \rightarrow T2 \rightarrow b$; $v_o = v_s$. At $\omega t = \pi$ current becomes zero and T1, T2 turn OFF (line commutation).
- **Negative half cycle (π to 2π):** b is positive; T3 and T4 are fired at $\omega t = \pi + \alpha$. Current flows $b \rightarrow T3 \rightarrow \text{load} \rightarrow T4 \rightarrow a$, in the **same direction** through the load; $v_o = -v_s$.
- Thus the output is a controlled full-wave DC voltage. Increasing α reduces the output.

Average output voltage: $V_{dc} = (V_m/\pi)(1 + \cos \alpha)$

$$V_m = \sqrt{2} \times 230 = 325.27 \text{ V}$$

$$V_{dc} = (325.27/\pi)(1 + \cos 45^\circ) = \mathbf{176.75 \text{ V}}$$

$$I_{dc} = V_{dc}/R = 176.75/20 = \mathbf{8.84 \text{ A}}$$

(Check: numerical average of the plotted waveform = 176.75 V)

(Waveform 1 M, explanation 1 M, V_{dc} 1 M, I_{dc} 1 M)

Q.3

a) RC half-wave triggering; $\alpha > 90^\circ$

4 M

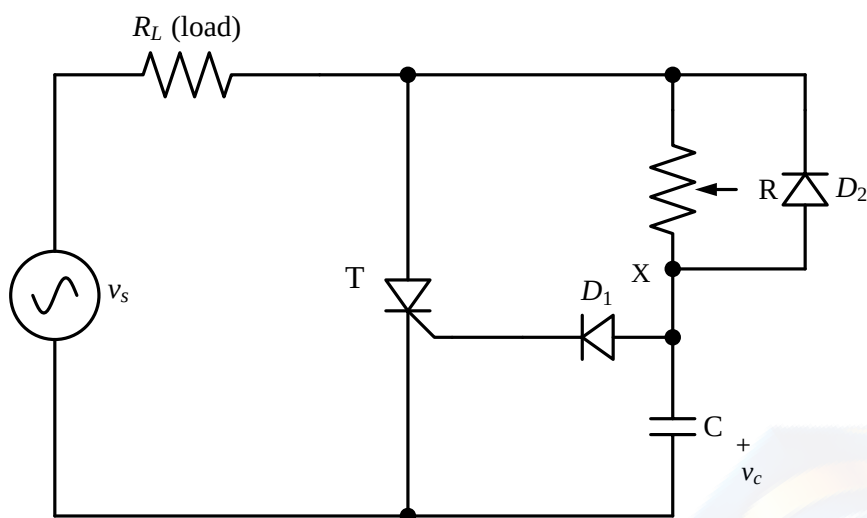


Fig.: RC half-wave firing circuit of SCR

- **Negative half cycle:** diode D_2 conducts and capacitor C charges to the negative peak $-V_m$ (lower plate positive). D_1 blocks reverse voltage to the gate.
- **Positive half cycle:** after the negative peak, C starts charging through R from $-V_m$ towards the positive supply voltage. The capacitor voltage lags the supply voltage.
- When v_c reaches the gate trigger voltage ($V_{gt} + \text{diode drop of } D_1$), gate current flows through D_1 and the **SCR fires**. After this the SCR voltage falls to ≈ 1 V and C stops charging.
- Increasing R (time constant RC) delays the instant at which v_c reaches V_{gt} , so α increases. Because of the RC phase shift, **α can be varied from about 0° to nearly 180° .**
- For reliable firing RC is chosen such that $RC \geq 1.3 (T/2)$, where T is the supply period.

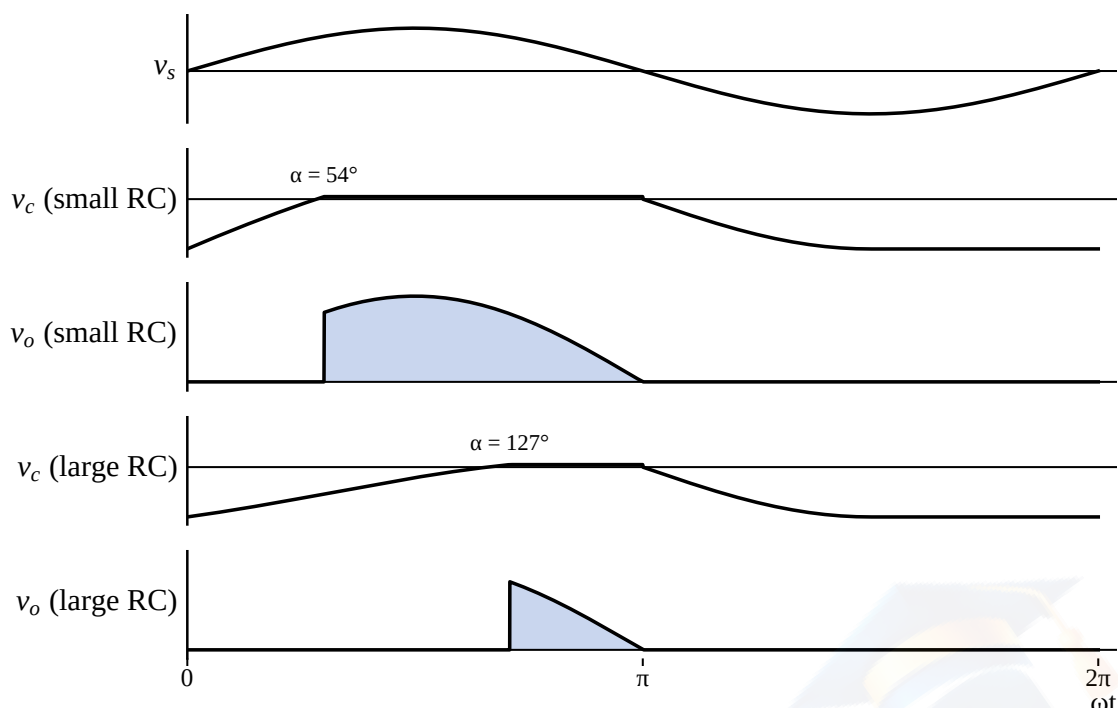


Fig.: Waveforms of RC half-wave firing circuit — α can be varied beyond 90° (up to nearly 180°)

Plotted example: small RC $\rightarrow \alpha \approx 54^\circ$, large RC $\rightarrow \alpha \approx 127^\circ$ (beyond 90° , not possible with R firing).

How $\alpha > 90^\circ$ is possible: the capacitor voltage lags the supply voltage and starts charging from $-V_m$. With large RC it reaches the trigger voltage even after the supply peak (90°), so the SCR can be fired late in the half cycle (up to nearly 180°). In R firing the gate voltage is in phase with the supply, so α cannot exceed 90° .

(Circuit 1 M, waveforms 1 M, explanation 1 M, reason 1 M)

b) UJT relaxation oscillator triggering

4 M

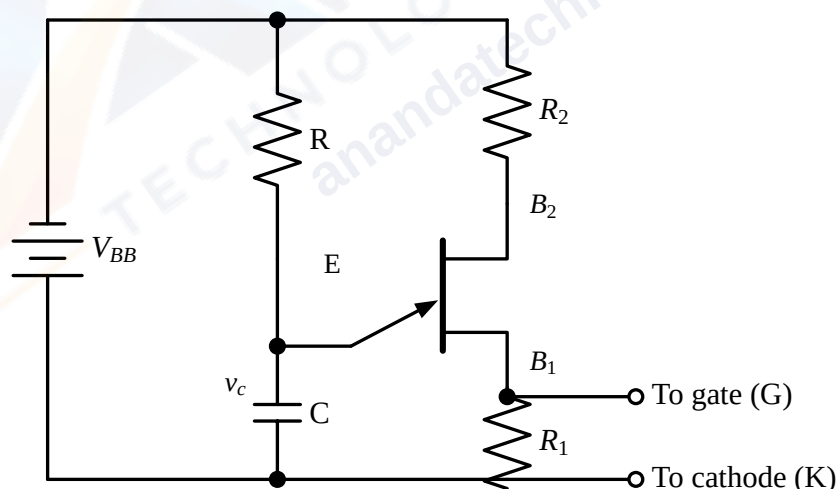


Fig.: UJT relaxation oscillator used for triggering SCR

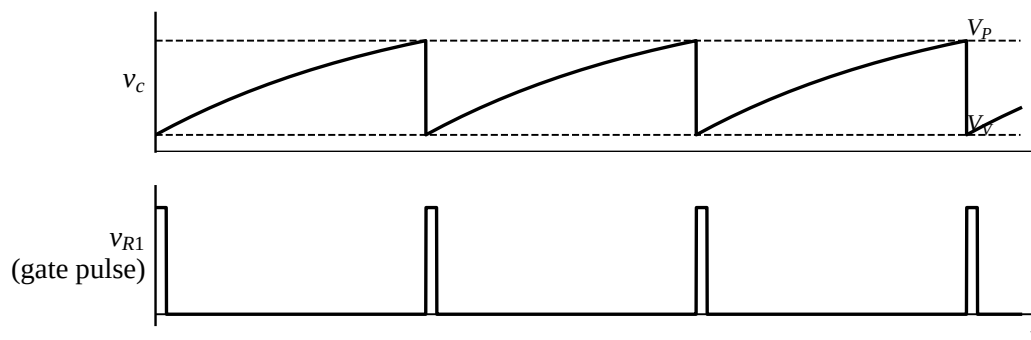


Fig.: Capacitor voltage and output pulses of UJT relaxation oscillator

- Capacitor C charges through R from V_{BB} . When v_c reaches the **peak point voltage** $V_P = \eta V_{BB} + V_D$, the UJT turns ON (emitter–B1 resistance falls).
- C discharges rapidly through the emitter and R_1 , producing a **sharp voltage pulse across R_1** which is applied to the SCR gate (directly or through a pulse transformer).
- When v_c falls to the valley voltage V_V , the UJT turns OFF and C charges again — a train of pulses is produced.
- Period $T = RC \ln[1/(1 - \eta)]$; changing R changes the pulse timing and hence the firing angle. For phase control the UJT supply is taken from the same AC supply (rectified and zener-clipped) for synchronisation.

Example: $R = 10 \text{ k}\Omega$, $C = 0.1 \text{ }\mu\text{F}$, $\eta = 0.63 \rightarrow T = RC \ln[1/(1 - \eta)] = 10^{-3} \times \ln(1/0.37) = \mathbf{0.994 \text{ ms}}$, $f \approx \mathbf{1006 \text{ Hz}}$

(Circuit 1 M, waveforms 1 M, working 2 M)

c) Half controlled vs fully controlled bridge

4 M

Point	Half controlled (semi-converter)	Fully controlled (full converter)
Devices	2 SCRs + 2 diodes	4 SCRs
Quadrant of operation	One quadrant (V_{dc} and I_{dc} positive)	Two quadrant (rectification and inversion)
Average output voltage	$V_{dc} = (V_m/\pi)(1 + \cos \alpha)$	$V_{dc} = (2V_m/\pi) \cos \alpha$ (continuous current)
Negative output voltage	Not possible (freewheeling action)	Possible for $\alpha > 90^\circ$ with inductive load
Input power factor	Better	Poorer at large α
Firing circuits / cost	Two firing circuits; cheaper	Four firing circuits; costlier

(Any four points, 1 M each)

d) Step-up chopper; $V_s = 48 \text{ V}$, $D = 0.6$

4 M

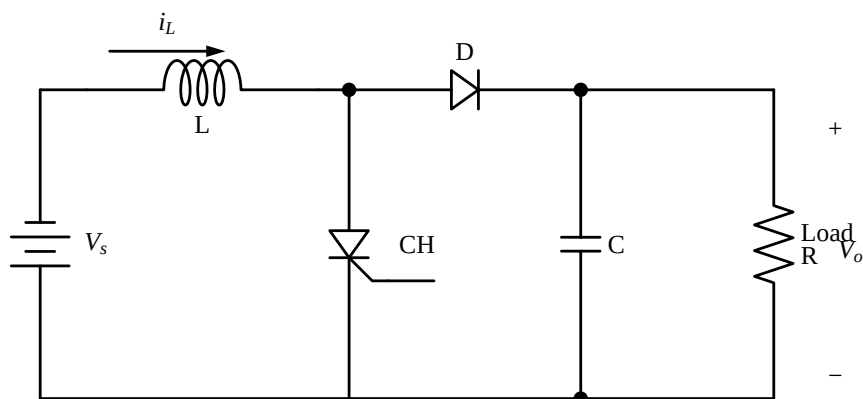


Fig.: Step-up (boost) chopper

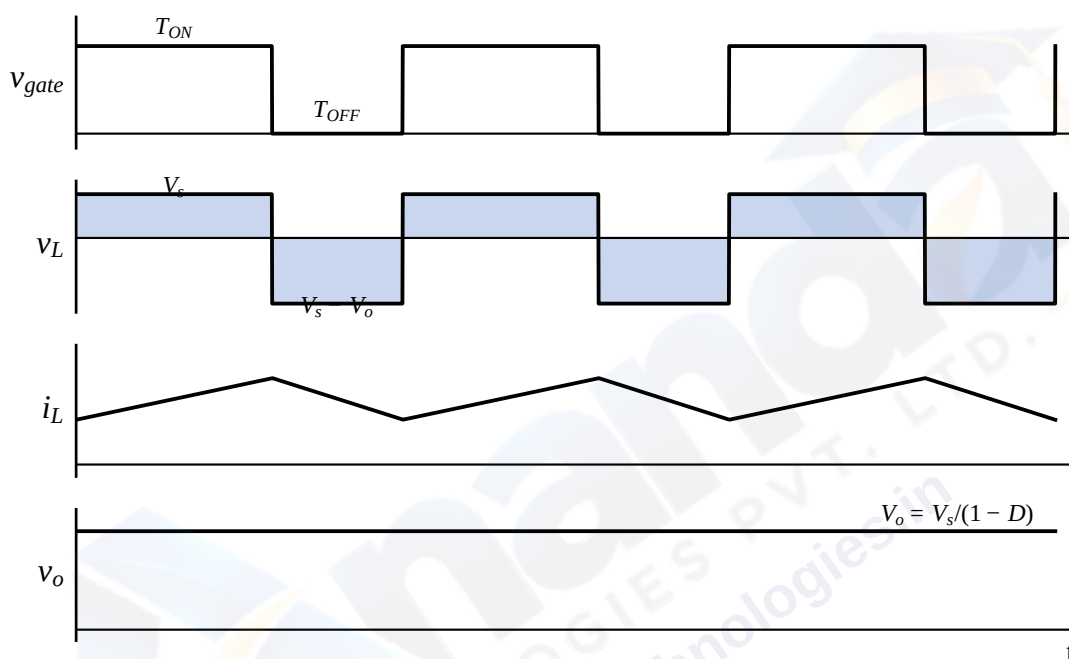


Fig.: Waveforms of step-up chopper ($D = 0.6$)

- An inductor L is connected in series with the supply; chopper CH is connected across the supply–inductor combination and diode D feeds the load and capacitor C .
- **CH ON (T_{ON}):** the supply is short-circuited through L ; current i_L rises and energy is stored in L ($v_L = V_s$). D is reverse biased and C supplies the load.
- **CH OFF (T_{OFF}):** the inductor voltage reverses ($L \, di/dt$) and **adds to the supply voltage**; current flows through D to C and the load. Load voltage $V_o = V_s + L \, di/dt$, i.e. more than V_s .
- Volt-second balance of L : $V_s T_{ON} = (V_o - V_s) T_{OFF}$.

Output voltage: $V_o = V_s \cdot T / (T - T_{ON}) = V_s / (1 - D)$ ($V_o > V_s$)

$$V_o = V_s / (1 - D) = 48 / (1 - 0.6) = 120 \text{ V}$$

(Circuit 1 M, working 2 M, calculation 1 M)

Q.4

a) 3- ϕ fully controlled bridge, R load, $\alpha = 90^\circ$; 400 V

4 M

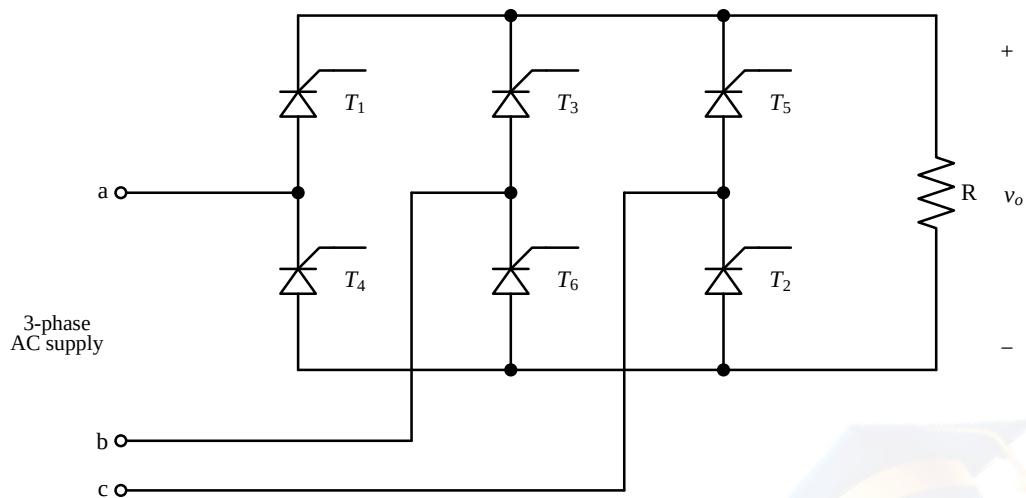


Fig.: Three phase fully controlled bridge rectifier with R load

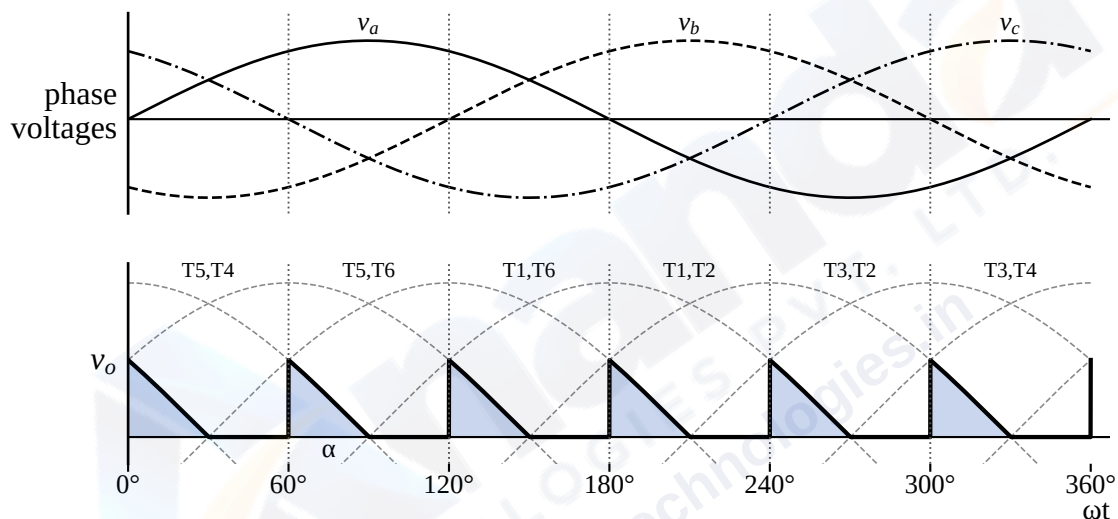


Fig.: Output voltage of 3- ϕ fully controlled bridge with R load ($\alpha = 90^\circ$); thin dashed curves are the six line voltages

For $\alpha > 60^\circ$ with R load each line voltage becomes zero before the next pair is fired, so the output current becomes **discontinuous** (zero gaps in v_o). Each pair conducts only from $30^\circ + \alpha$ to 180° of its line voltage.

$$V_{dc} = (3V_{ml}/\pi)[1 + \cos(60^\circ + \alpha)] \text{ for } 60^\circ \leq \alpha \leq 120^\circ$$

$$V_{ml} = \sqrt{2} \times 400 = 565.69 \text{ V}$$

$$V_{dc} = (3 \times 565.69/\pi)[1 + \cos 150^\circ] = 540.19 \times 0.1340 = \mathbf{72.37 \text{ V}}$$

(numerical average of computed waveform = 72.37 V)

(Circuit 1 M, waveform 2 M, calculation 1 M)

b) Pulse width modulator; multiple pulse modulation

4 M

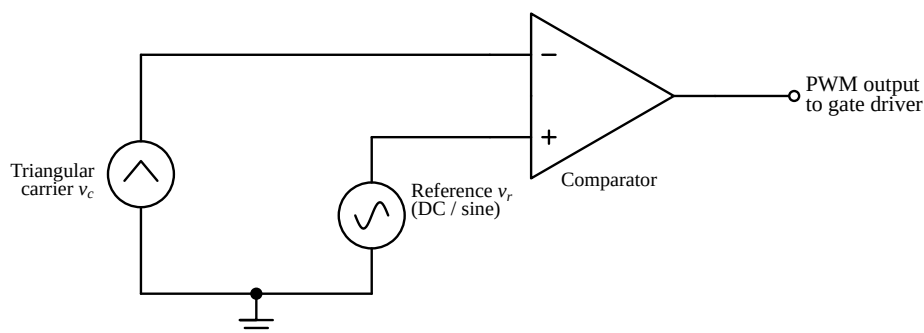


Fig.: Pulse width modulator — comparator generating PWM gate pulses

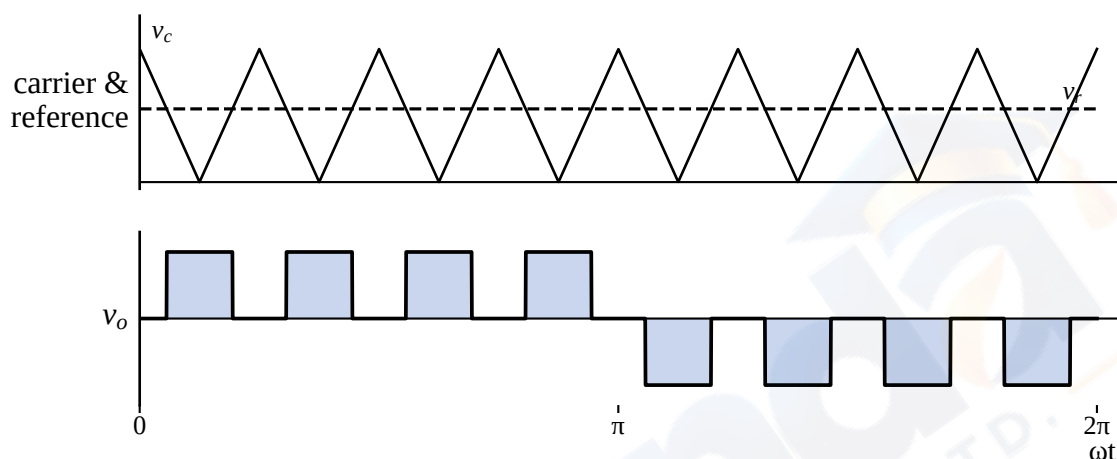


Fig.: Multiple pulse modulation (4 pulses per half cycle)

- A triangular carrier v_c is compared with a DC (square) reference v_r in a comparator; the comparator output is HIGH when $v_r > v_c$. These pulses (steered to the switches in alternate half cycles) form the inverter output.
- In **multiple pulse modulation** several equal-width, equally spaced pulses are produced in each half cycle. Number of pulses per half cycle $p = f_c / (2f_o)$.
- Output voltage is controlled by varying the reference amplitude (pulse width); output frequency by the reference / switching frequency.
- Compared with single pulse modulation, lower order harmonics are reduced, but switching losses are higher.

(Circuit 1 M, waveforms 1 M, explanation 2 M)

c) Constant frequency control; 1 kHz, 120 V → 90 V

4 M

In **constant frequency (PWM) control** the chopping period T (i.e. frequency) is kept constant and the ON time T_{ON} is varied from 0 to T . Thus the duty cycle $D = T_{ON}/T$ and $V_o = D \cdot V_s$ are varied.

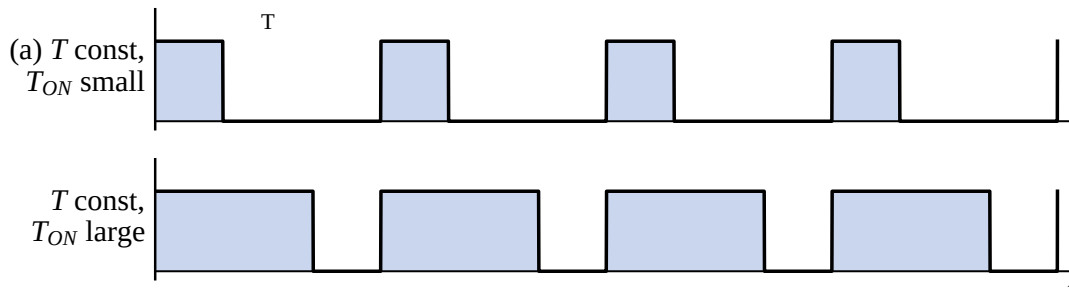


Fig.: Constant frequency control — T constant, T_{ON} varied

Advantages: harmonic frequencies are fixed, so filter design is easy; most widely used.

$$T = 1/f = 1/1000 = 1 \text{ ms}; D = V_o/V_s = 90/120 = 0.75$$

$$T_{ON} = D \times T = 0.75 \times 1 \text{ ms} = \mathbf{0.75 \text{ ms}}; T_{OFF} = T - T_{ON} = \mathbf{0.25 \text{ ms}}$$

(Explanation with waveform 2 M, calculation 2 M)

d) Solar power system

4 M

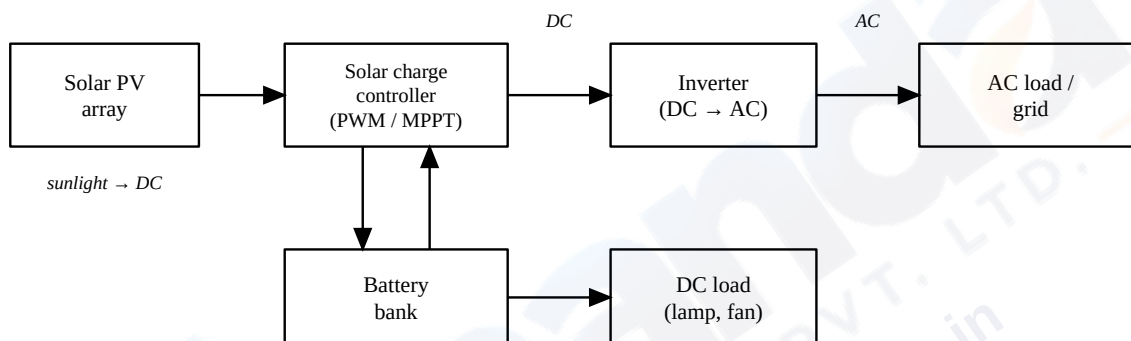


Fig.: Block diagram of solar PV power system with charge controller

- **Solar PV array:** series–parallel connected PV modules convert sunlight directly into DC electricity.
- **Solar charge controller:** regulates the voltage/current from the PV array to charge the battery safely; prevents **overcharging**, **deep discharge** and **reverse current** from battery to panel at night. Types: ON-OFF (series / shunt), PWM and MPPT.
- **Battery bank:** stores energy for use at night or on cloudy days.
- **Inverter:** converts DC into 230 V, 50 Hz AC for AC loads or grid connection. DC loads (LED lamps, DC fans) can be fed directly.

(Block diagram 2 M, explanation 2 M)

e) AC to AC converter using DC link; applications

4 M

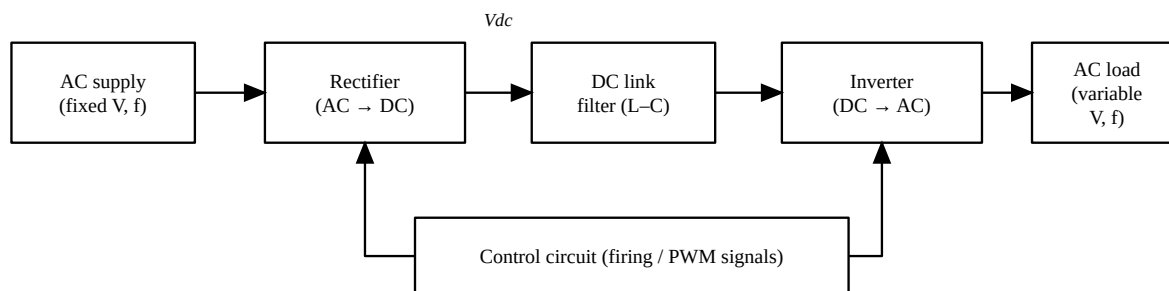


Fig.: Block diagram of AC to AC converter using DC link

- **Rectifier:** converts the fixed voltage, fixed frequency AC supply into DC (diode or SCR bridge).
- **DC link:** an L-C filter smooths the rectified voltage; the capacitor holds a steady DC voltage (V_{dc}) and decouples the two converters.
- **Inverter:** converts the DC link voltage into AC of the **required voltage and frequency** using PWM switching of IGBTs/MOSFETs.
- **Control circuit:** generates firing pulses for the rectifier and PWM pulses for the inverter according to the reference (speed / frequency).
- Thus AC of one frequency is converted to AC of another frequency in two stages (AC → DC → AC); output frequency is independent of input frequency.

Applications: variable frequency drives (speed control of induction motors), wind power generation (variable frequency generator output to 50 Hz grid), UPS, induction heating, HVDC back-to-back links.

(Block diagram 2 M, explanation 1 M, applications 1 M)

Q.5

a) Layer construction of SCR and V-I characteristics; I_L , I_H

6 M

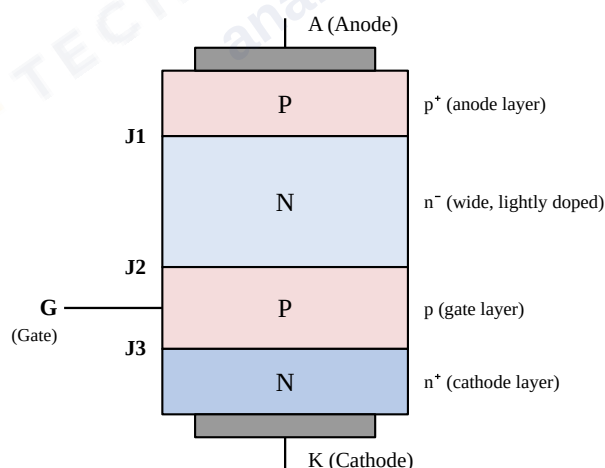


Fig.: Construction (layer structure) of SCR

SCR is a **four-layer p-n-p-n** device with **three junctions J1, J2, J3** and three terminals: anode (outer p layer), cathode (outer n layer) and gate (inner p layer near the cathode).

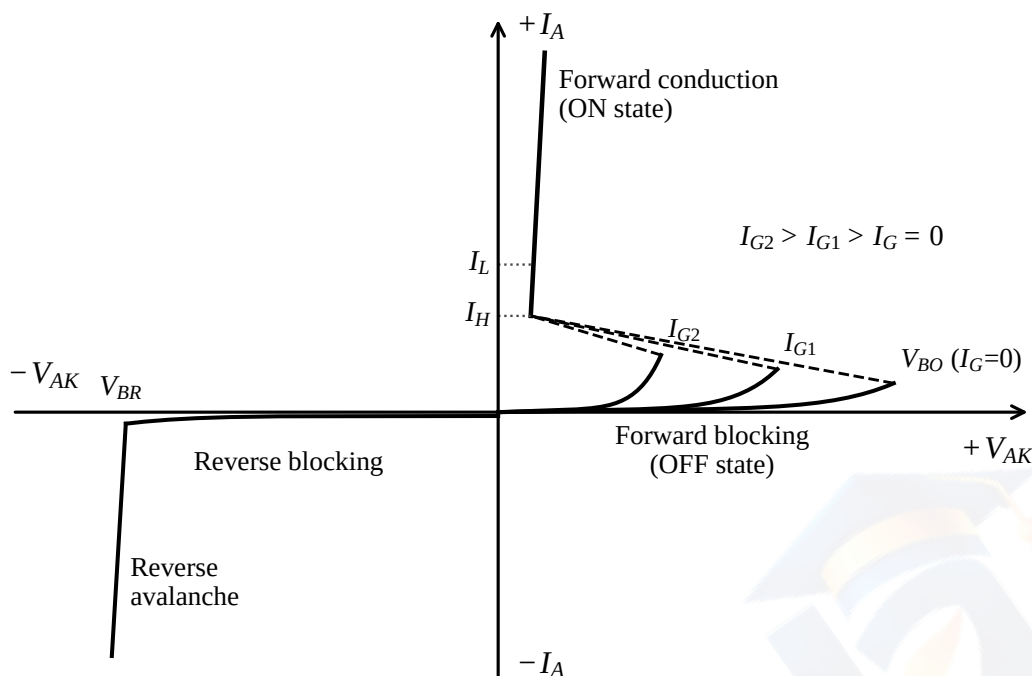


Fig.: V-I characteristics of SCR

- **Reverse blocking region:** Anode is negative w.r.t. cathode. Junctions J1 and J3 are reverse biased, so only a small reverse leakage current flows. If reverse voltage exceeds the reverse breakdown voltage V_{BR} , avalanche breakdown occurs and the SCR may be damaged.
- **Forward blocking (OFF) region:** Anode is positive w.r.t. cathode, gate open. J1 and J3 are forward biased but J2 is reverse biased, so only a small forward leakage current flows. The SCR is OFF.
- **Forward conduction (ON) region:** When the forward voltage reaches the forward breakover voltage V_{BO} , J2 breaks down and the SCR turns ON. The voltage across it falls to about 1–2 V and the current is limited only by the load.
- **Effect of gate current:** When gate current is applied, the SCR turns ON at a lower forward voltage. Larger gate current $\rightarrow$ smaller breakover voltage ($I_{G2} > I_{G1}$ gives lower V_{BO}).

Latching current (I_L): The minimum anode current that must flow through the SCR immediately after turn-ON (when the gate pulse is removed) to keep it latched in the ON state.

Holding current (I_H): The minimum anode current required to keep the SCR in the ON state. If the anode current falls below I_H , the SCR turns OFF. Normally $I_L \approx 2$ to 3 times I_H .

(Construction 1 M, characteristics 2 M, explanation 2 M, definitions 1 M)

b) R firing circuit; waveforms for R minimum and maximum

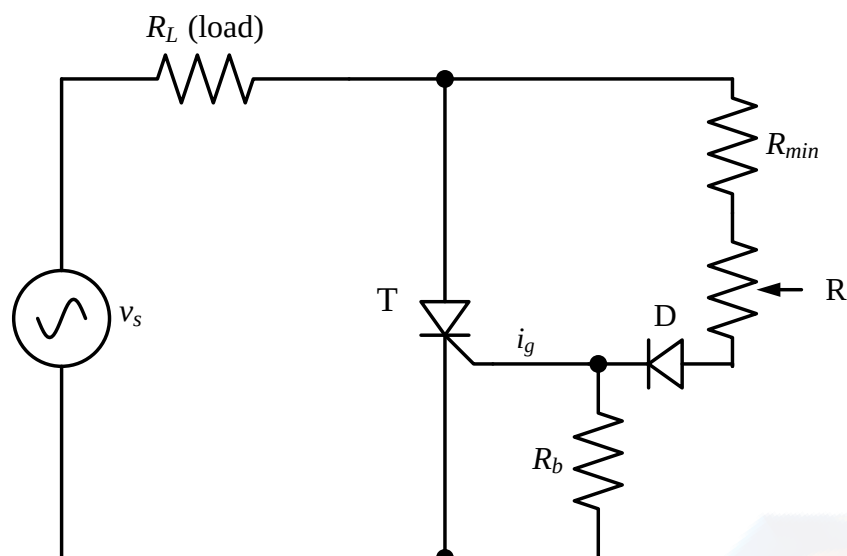


Fig.: Resistance (R) firing circuit of SCR

- R_{min} limits gate current when $R = 0$; variable R sets the firing angle; diode D blocks reverse gate voltage; R_b limits gate voltage.
- In the positive half cycle gate current $i_g = v_s / (R_{min} + R + \text{load})$ rises with the supply. The SCR fires when i_g reaches I_{gt} .
- **R minimum:** gate current reaches I_{gt} very early, so α is small ($\approx 25^\circ$ in the plotted case) and almost the full half cycle appears across the load.
- **R maximum:** the peak gate current just equals I_{gt} , so the SCR fires at the peak, $\alpha = 90^\circ$; the load gets only the second quarter of the positive half cycle. R larger than this — SCR does not fire.
- Hence the firing angle range of R triggering is 0° to 90° .

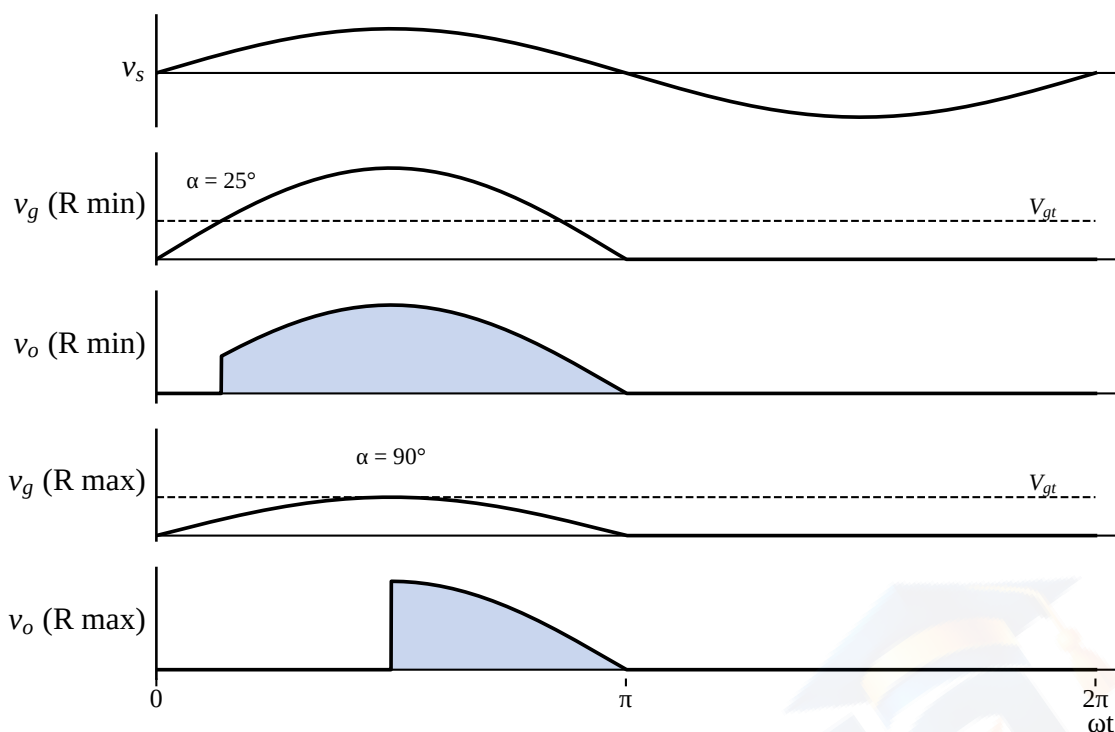


Fig.: R firing circuit waveforms — R minimum (α small) and R maximum ($\alpha = 90^\circ$)

(Circuit 2 M, explanation 2 M, waveforms 2 M)

c) 1- ϕ half wave controlled rectifier with R-L load; effect of FWD

6 M

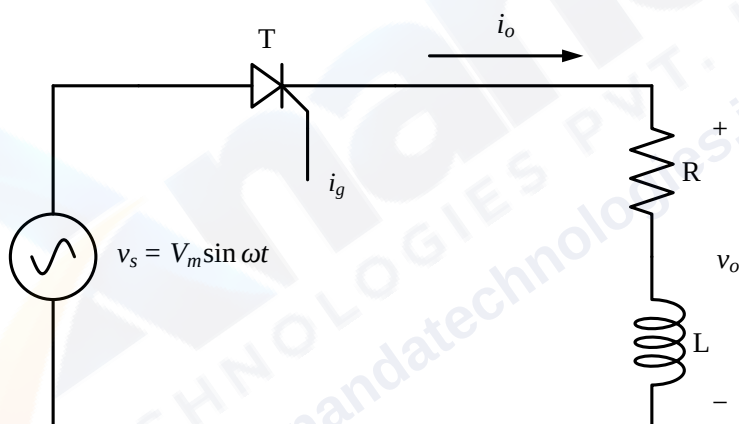


Fig.: Single phase half wave controlled rectifier with RL load

- SCR is fired at $\omega t = \alpha$ in the positive half cycle; $v_o = v_s$. Because of inductance the current rises slowly, reaches a maximum and starts decreasing.
- At $\omega t = \pi$ the supply becomes negative but the inductor voltage ($L di/dt$) keeps the SCR forward biased, so the SCR **continues to conduct up to the extinction angle β ($> \pi$)** and the output voltage becomes negative during π to β .
- At β the current becomes zero and the SCR turns off. (For $\alpha = 45^\circ$ and load angle $\phi = 60^\circ$, $\beta = 242^\circ$ — computed.) $V_{dc} = (V_m/2\pi)(\cos \alpha - \cos \beta)$.

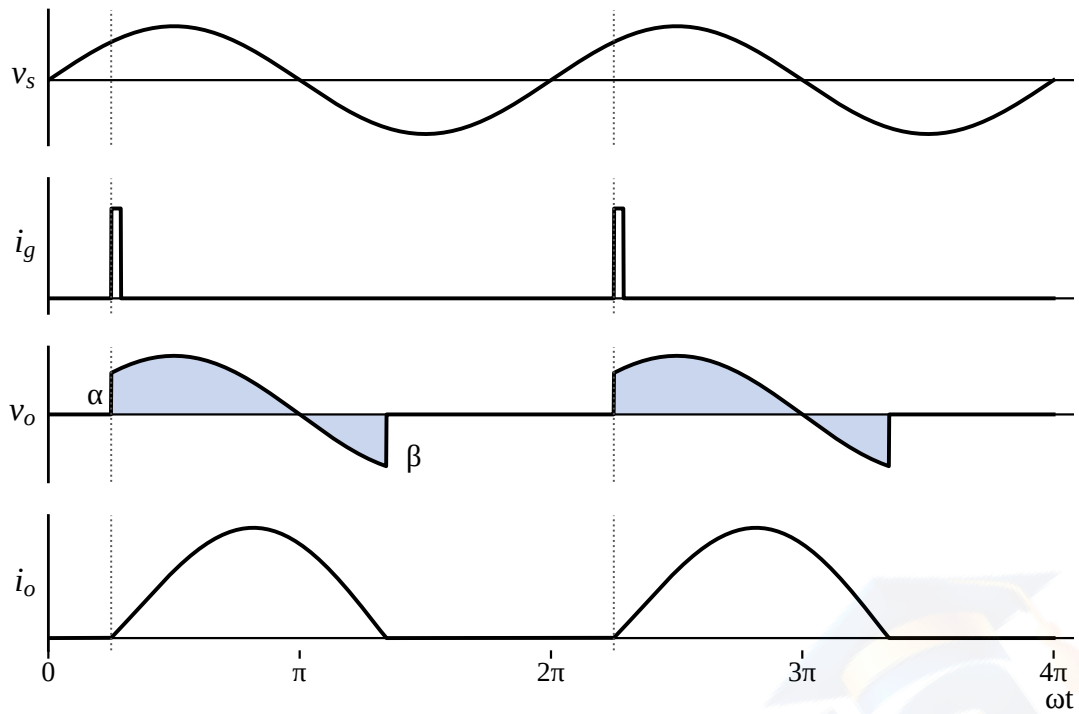


Fig.: Waveforms — R-L load ($\alpha = 45^\circ$); SCR conducts beyond π up to β because of L

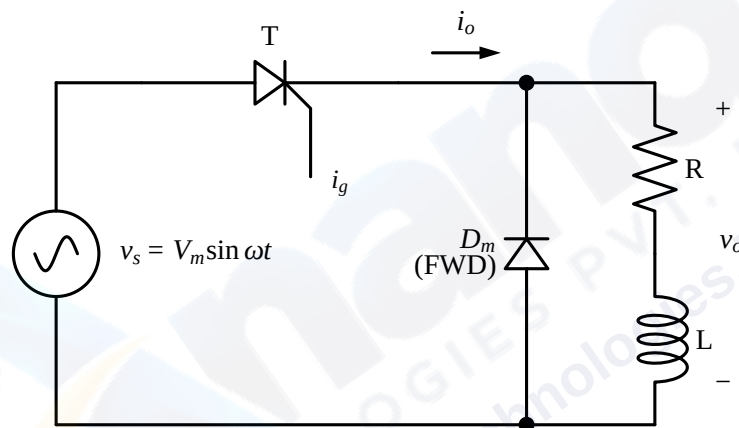


Fig.: Single phase half wave controlled rectifier with RL load and freewheeling diode

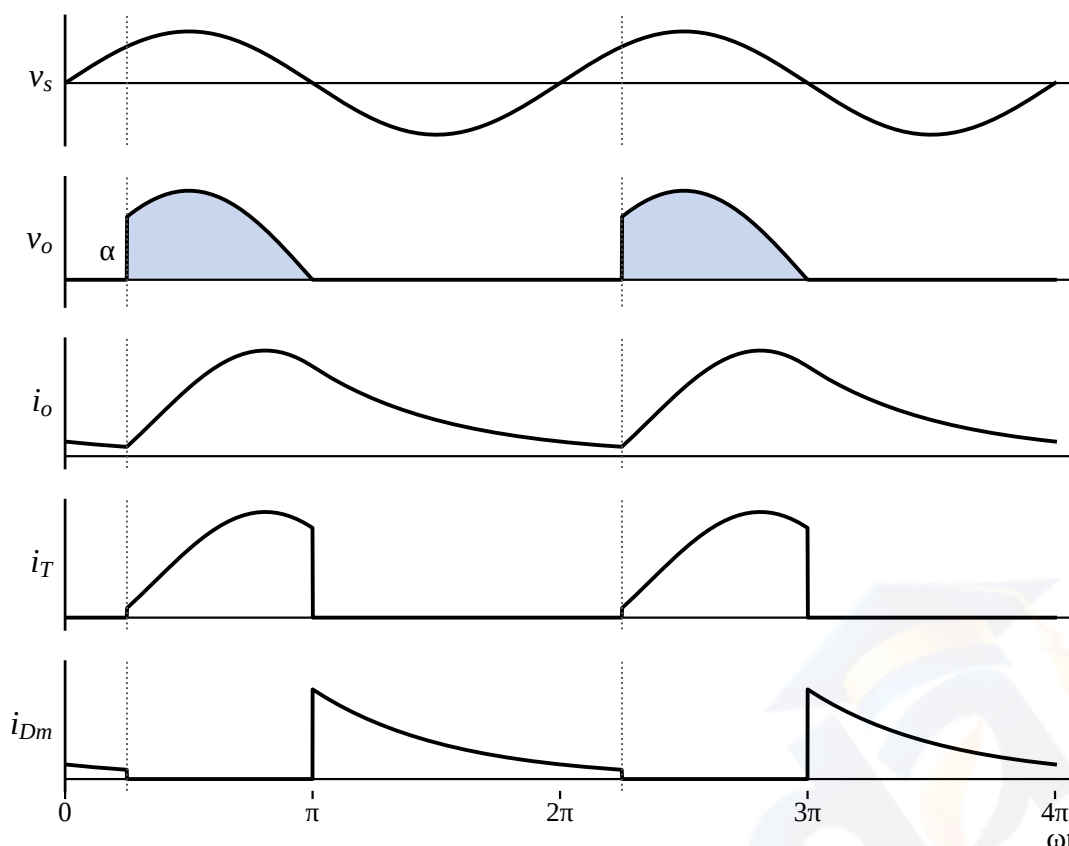


Fig.: Waveforms with freewheeling diode, R-L load ($\alpha = 45^\circ$): no negative part in output voltage

- **Effect of freewheeling diode:** at $\omega t = \pi$ the FWD D_m becomes forward biased and takes over the load current; the SCR turns off at π .
- The **negative part of v_o is removed**, so V_{dc} increases to $(V_m/2\pi)(1 + \cos \alpha)$.
- Load current decays through D_m (freewheeling) and becomes smoother; energy of L goes to the load instead of the supply.

(Circuit 1 M, waveforms without FWD 2 M, with FWD 2 M, explanation 1 M)

Q.6

a) Symbols and V-I characteristics of power MOSFET, TRIAC, IGBT

6 M

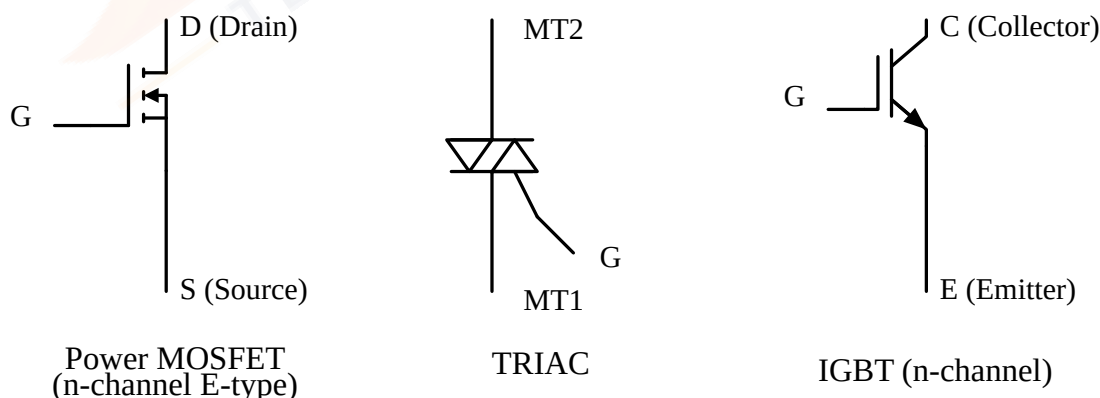


Fig.: Symbols of power MOSFET, TRIAC and IGBT

(i) Power MOSFET: drain current I_D is controlled by V_{GS} ; no current below $V_{GS(th)}$; ohmic region at low V_{DS} and active (saturation) region where I_D is nearly constant.

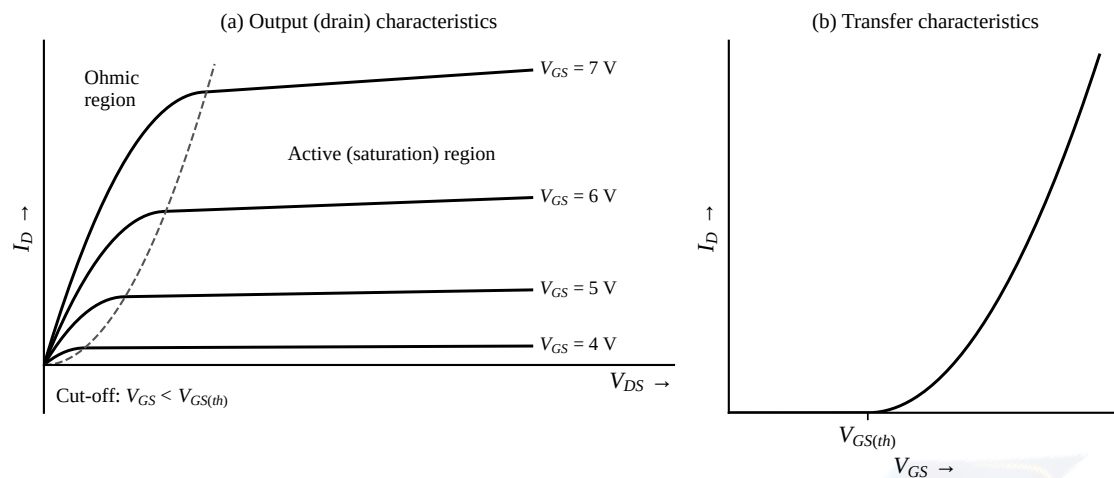


Fig.: Characteristics of n-channel enhancement power MOSFET

(ii) TRIAC: identical characteristics in quadrant I (MT2 positive) and quadrant III (MT2 negative); gate current reduces the breakover voltage.

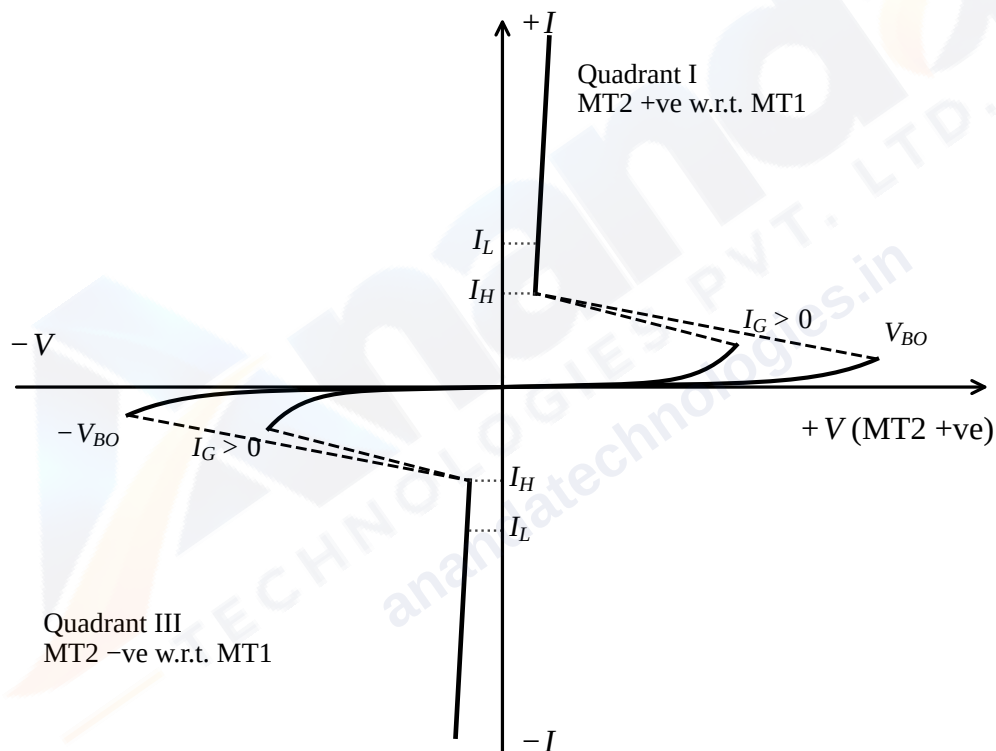


Fig.: V-I characteristics of TRIAC

(iii) IGBT: collector current I_C is controlled by V_{GE} ; curves start after ≈ 0.7 V (p^+ injecting junction); low $V_{CE(sat)}$ in ON state.

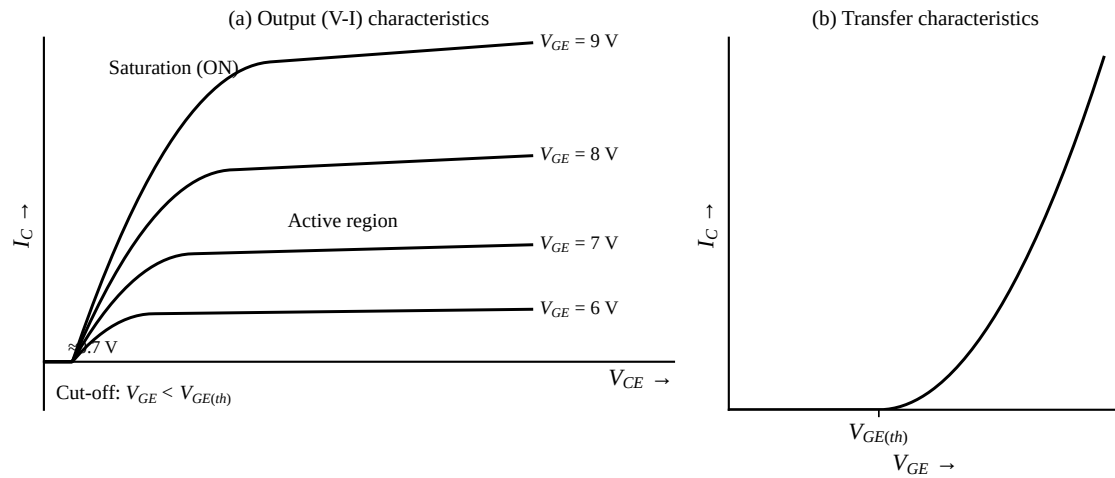


Fig.: Characteristics of IGBT

(Each symbol with labelled characteristics 2 M)

b) 1- ϕ full bridge inverter with R load; full vs half bridge

6 M

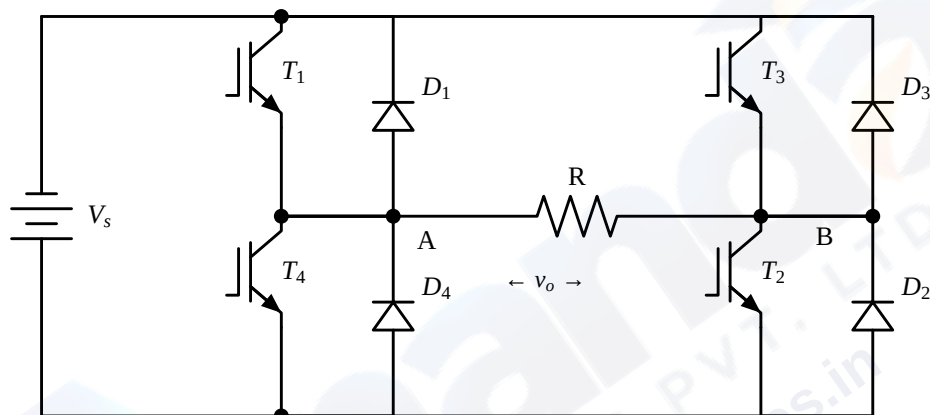


Fig.: Single phase full bridge inverter with R load

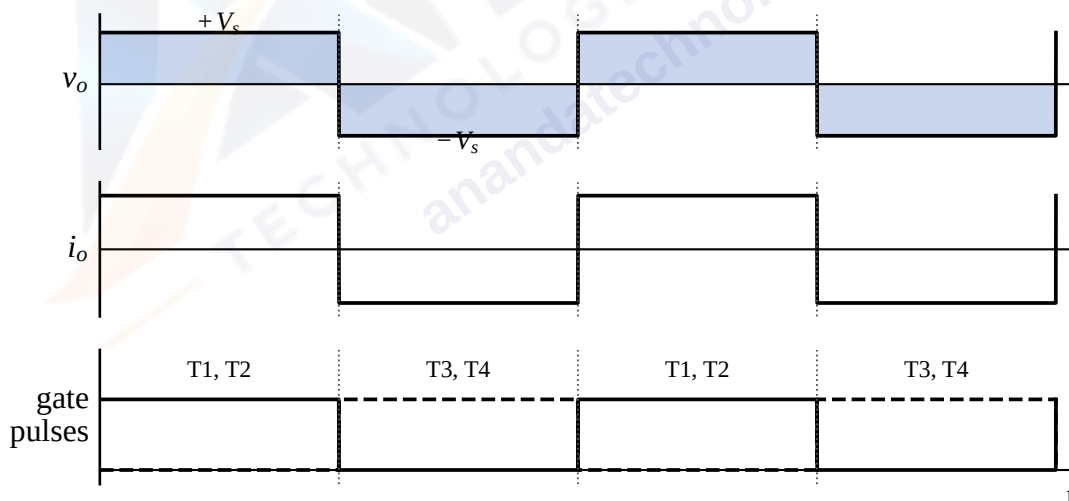


Fig.: Output waveforms of 1- ϕ full bridge inverter with R load

- The full bridge inverter has **four switches T1–T4** with feedback diodes D1–D4 and a two-wire DC supply V_s . The load is connected between the leg mid-points A and B.
- $0 < t < T/2$: T1 and T2 are ON; A is connected to $+V_s$ and B to $-$; $v_o = +V_s$.
- $T/2 < t < T$: T1, T2 are turned OFF and T3, T4 ON; the load voltage reverses: $v_o = -V_s$.

- Output is a square wave of amplitude V_s (double that of half bridge for the same supply).

Frequency is varied by changing the switching rate.

RMS output voltage = V_s ; RMS value of fundamental $V_{o1} = 4V_s/(\pi\sqrt{2}) = 0.9 V_s$.

Point	Half bridge inverter	Full bridge inverter
Number of switches	2	4
DC supply	Three-wire (centre tapped / two sources)	Two-wire
Output voltage amplitude	$V_s/2$	V_s (double)
Fundamental RMS output	$0.45 V_s$	$0.9 V_s$
Power output / cost	Low power, cheaper	Higher power (4×), costlier

(Circuit 2 M, waveforms 1 M, working 1 M, comparison 2 M)

c) Speed control of fan using TRIAC (block diagram); advantages

6 M

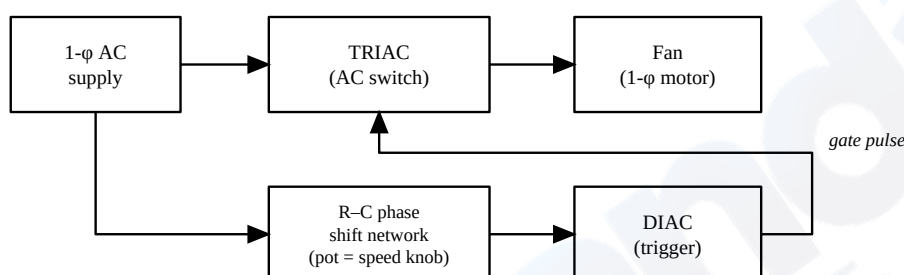


Fig.: Block diagram — speed control of fan using TRIAC

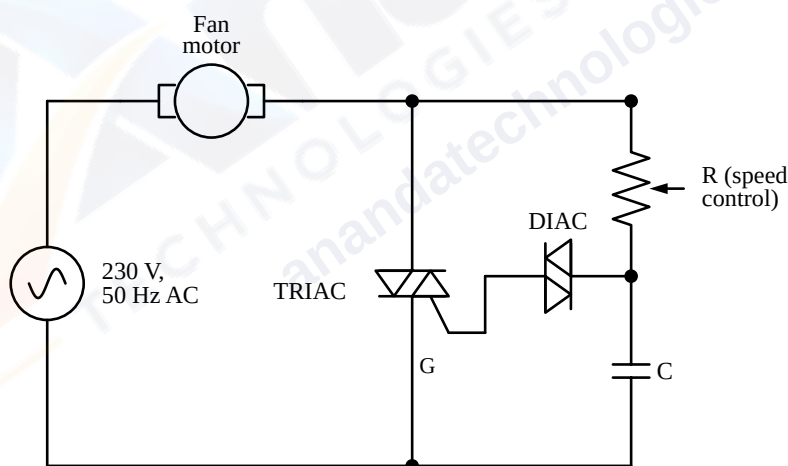


Fig.: Fan speed regulator using TRIAC and DIAC

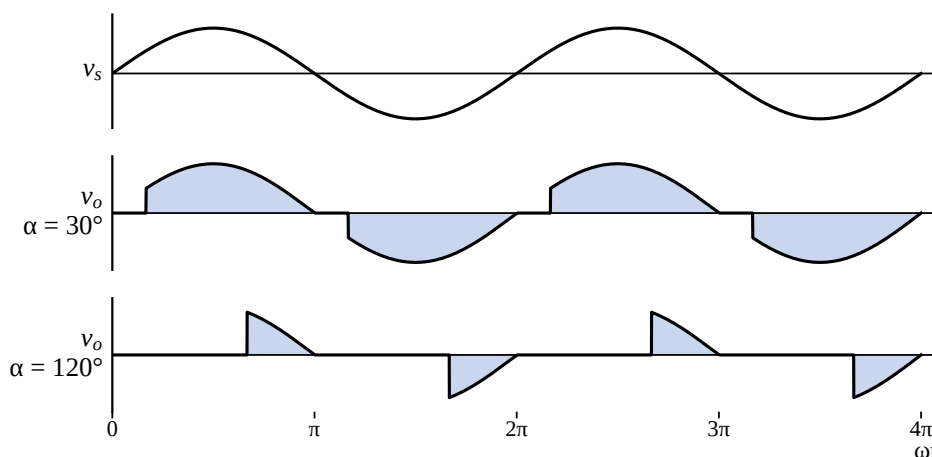


Fig.: Voltage across fan for two firing angles (small α = high speed, large α = low speed)

- The TRIAC is connected in series with the fan motor across the 230 V AC supply. An R-C network (R = speed control potentiometer) is connected across the TRIAC and a DIAC connects the R-C junction to the TRIAC gate.
- In each half cycle capacitor C charges through R. When the capacitor voltage reaches the **breakover voltage of the DIAC (≈ 30 V)**, the DIAC conducts and gives a gate pulse to the TRIAC.
- The TRIAC turns ON and applies the supply voltage to the fan for the rest of the half cycle; it turns OFF at current zero. Since TRIAC and DIAC are bidirectional, this happens in **both half cycles**.
- **Increasing R** $\rightarrow$ capacitor charges slowly $\rightarrow$ firing angle α increases $\rightarrow$ RMS voltage across fan decreases $\rightarrow$ **speed decreases**. Decreasing R increases speed. Thus smooth (stepless) speed control is obtained.

Advantages over resistive regulator:

- Very small power loss — no voltage dropped in a resistor, so energy is saved (resistive regulator wastes power as heat at low speed).
- Smooth, stepless speed control.
- Small size, light weight and low cost.
- Long life — no sliding contacts.

(Block diagram 2 M, working 2 M, advantages 2 M)

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