

Analog Electronics (313324)

MSBTE K-Scheme · Model Question Paper — Set C · Model Answers

Q.1 Attempt any FIVE of the following:

10 marks

a) State the need of heat sink in a power amplifier.

2 M

Heat sink: A heat sink is a metal plate (usually aluminium, with fins, painted black) fixed in close thermal contact with the case of a power transistor to carry away the heat produced at the collector junction to the surrounding air.

- In a power amplifier the transistor dissipates large power ($P_D = V_{CE}I_C$), so its junction temperature rises.
- If the junction temperature exceeds the maximum rating ($\approx 150^\circ\text{C}$ for Si) the transistor is damaged; rise in temperature also causes **thermal runaway**.
- The heat sink increases the surface area, reduces the thermal resistance between case and air, and so allows the transistor to handle more power safely.

(Meaning 1 M, need / function 1 M)

b) Define: i) Input offset voltage ii) Input bias current

2 M

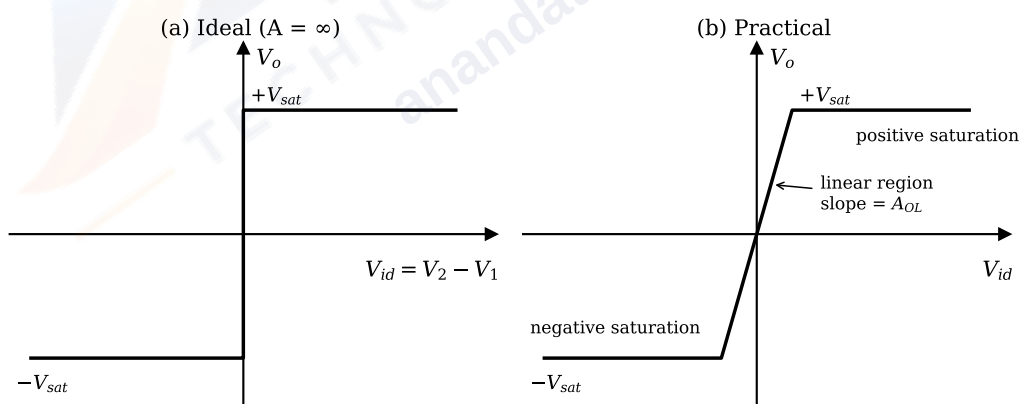
Input offset voltage (V_{io}): The differential DC voltage that must be applied between the two input terminals to make the output voltage zero.

Input bias current (I_B): The average of the currents flowing into the two input terminals when the output is zero: $I_B = (I_{B1} + I_{B2})/2$.

(Each definition 1 M)

c) Draw the ideal and practical transfer characteristics of op-amp.

2 M



Transfer characteristics of op-amp: (a) ideal (b) practical

Ideal op-amp: $A_{OL} = \infty$, so the output jumps between $\pm V_{sat}$ for any small V_{id} . Practical op-amp: linear region of slope A_{OL} for very small V_{id} ($\approx \pm 65 \mu\text{V}$ for $\pm 13 \text{ V}$ output with $A = 2 \times 10^5$), then saturation at about $\pm 13 \text{ V}$ (with $\pm 15 \text{ V}$ supply).

(Ideal 1 M, practical 1 M)

d) State the conditions required for sustained oscillations in an oscillator.

2 M

For sustained oscillations, the following two conditions (Barkhausen criteria) must be satisfied:

1. The magnitude of loop gain must be unity: $|A\beta| = 1$.
2. The total phase shift around the loop must be 0° or 360° (i.e. feedback must be positive).

(Each condition 1 M)

e) State two merits of active filters over passive filters.

2 M

- Active filters give gain (no signal loss); passive filters always attenuate.
- No inductors are needed, so they are small, light and cheap; also no loading problem due to high R_i and low R_o of op-amp.

(Any two, 1 M each)

f) List two applications of current to voltage converter.

2 M

- Converting the output current of a photodiode / photo-detector into voltage.
- Converting the current output of a DAC (digital-to-analog converter) into voltage.
- Current-to-voltage conversion in sensors (e.g. current transducers) and current measuring instruments.

(Any two, 1 M each)

g) Write the function of: i) IC 555 ii) IC 565

2 M

IC 555: a timer IC used to produce accurate time delays and oscillations — works as monostable multivibrator, astable multivibrator (square wave / clock generator), VCO, PWM, etc.

IC 565: a phase locked loop (PLL) IC — used for FM demodulation, frequency multiplication / synthesis, FSK demodulation, tracking filter.

(Each function 1 M)

Q.2 Attempt any THREE of the following:

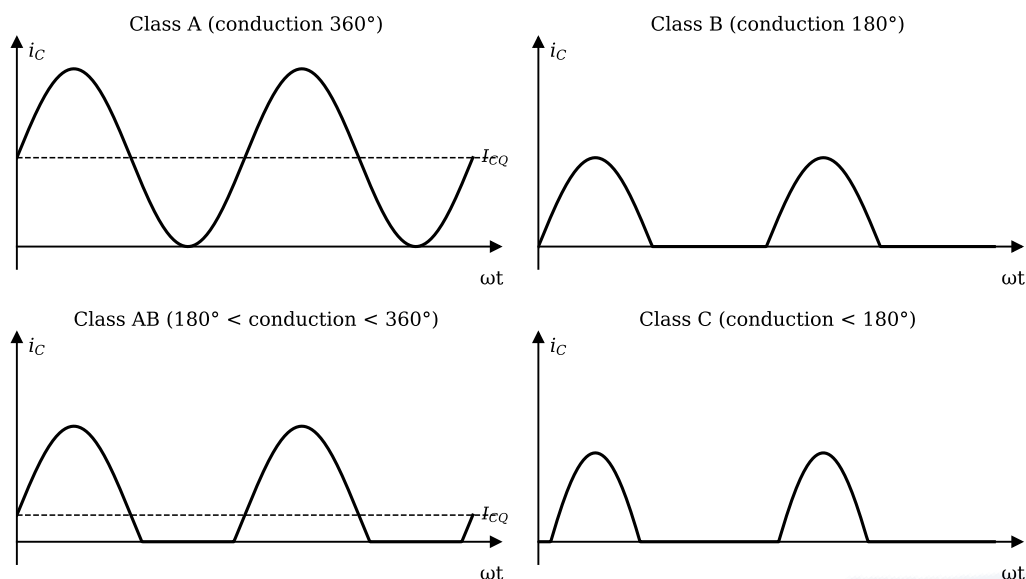
12 marks

a) Compare class A, class B, class AB and class C power amplifiers on the basis of: i)

Conduction angle ii) Efficiency iii) Q-point location iv) Applications

4 M

Parameter	Class A	Class B	Class AB	Class C
Conduction angle	360°	180°	Between 180° and 360°	Less than 180°
Maximum efficiency	25 % (resistive load), 50 % (transformer coupled)	78.5 %	Between 50 % and 78.5 %	More than 78.5 % (up to ≈ 95 %)
Position of Q-point	Centre of DC load line	At cut-off (on X-axis)	Slightly above cut-off	Below cut-off (beyond X-axis)
Applications	Small-signal / low power AF amplifier, driver stage	Push-pull AF output stage	Audio power output stages (PA systems, music systems)	RF tuned amplifiers, transmitters

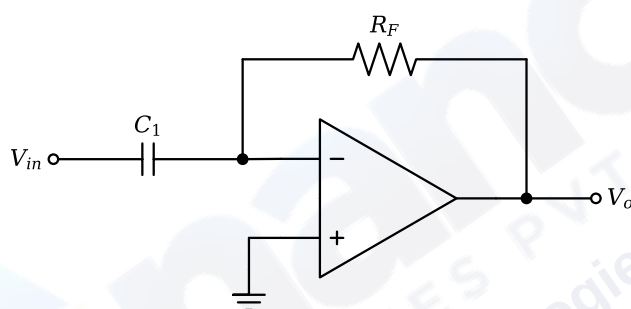


Collector current waveforms of class A, B, AB and C amplifiers

(Each correct parameter 1 M)

b) Draw the circuit of op-amp differentiator. Derive the expression for output voltage and draw its waveforms.

4 M



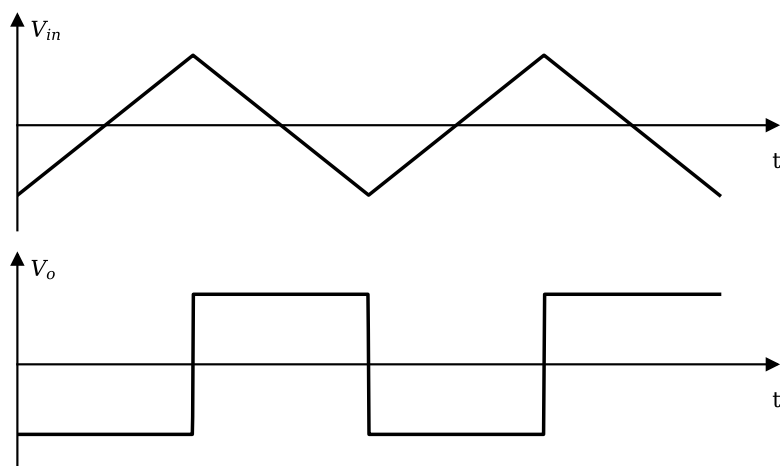
Basic op-amp differentiator

Derivation: The inverting input is at virtual ground and no current enters the op-amp, so the capacitor current flows through R_F :

$$i = C_1 \frac{d(V_{in} - 0)}{dt} = (0 - V_o)/R_F$$

$$V_o = -R_F C_1 \frac{dV_{in}}{dt}$$

The output is proportional to the rate of change of input. For a triangular input the output is a square wave; for a square wave input the output is a series of spikes. (Practical differentiator adds R_1 in series with C_1 and C_F across R_F to limit high-frequency gain and noise.)



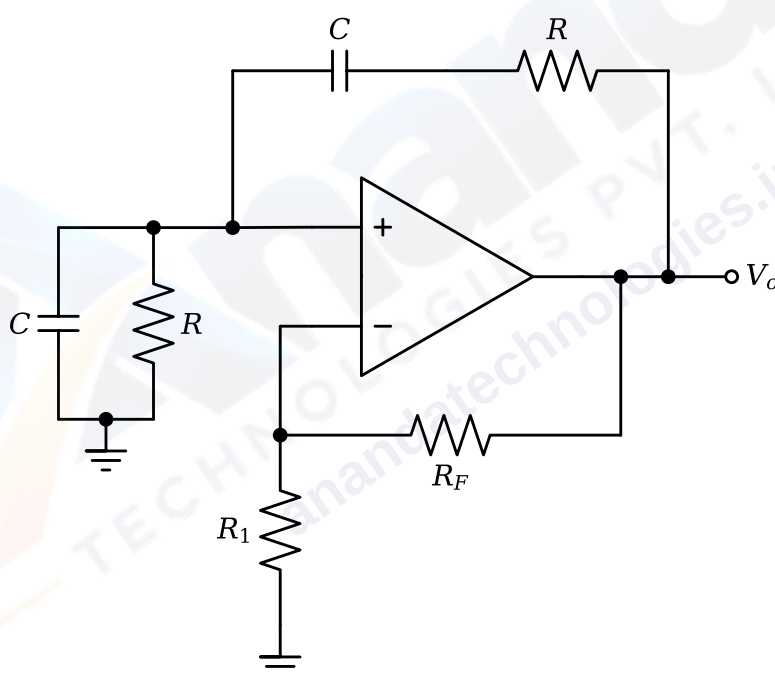
Differentiator: triangular input gives square wave output

(Circuit 1 M, derivation / working 2 M, waveforms 1 M)

c) Explain Wien bridge oscillator using op-amp. Calculate its frequency of oscillation for $R = 10 \text{ k}\Omega$ and $C = 0.01 \text{ }\mu\text{F}$.

4 M

Circuit: The op-amp works as a non-inverting amplifier (0° phase shift). The feedback network is a lead-lag network: series R–C from output to the (+) input and parallel R–C from (+) input to ground.



Wien bridge oscillator using op-amp

Working:

- At the frequency $f_0 = 1/(2\pi RC)$, the lead-lag network gives 0° phase shift and feedback factor $\beta = 1/3$.
- The non-inverting amplifier gain $A = 1 + R_F/R_1$ must be ≥ 3 , i.e. $R_F \geq 2R_1$, so that $A\beta = 1$.
- Total phase shift = 0° (amplifier) + 0° (network) = 0° , hence sustained sine wave output at f_0 .

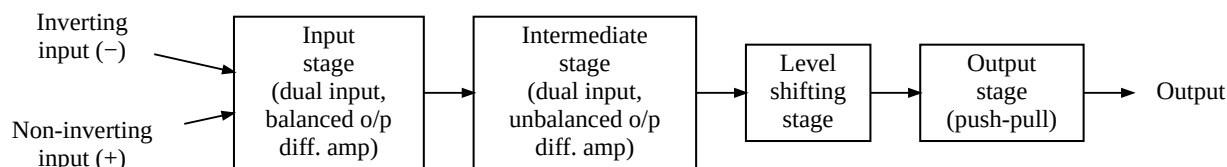
$$f_0 = 1 / (2\pi RC)$$

Calculation: $R = 10 \text{ k}\Omega$, $C = 10 \text{ nF}$: $f_o = 1/(2\pi \times 10000 \times 10 \times 10^{-9}) = 1.592 \text{ kHz}$. Take $R_1 = 10 \text{ k}\Omega$, $R_F = 2R_1 = 20 \text{ k}\Omega$ (slightly more for start-up).

(Circuit 2 M, working 1 M, frequency 1 M)

d) Draw the block diagram of op-amp. Write the function of each block.

4 M



Block diagram of op-amp

- **Input stage:** dual input, balanced output differential amplifier. It provides most of the voltage gain and decides the input resistance (high R_i) and CMRR.
- **Intermediate stage:** dual input, unbalanced (single-ended) output differential amplifier, driven by the input stage. It gives additional voltage gain.
- **Level shifting stage:** emitter follower / constant current source circuit which shifts the DC level at the output of the intermediate stage down to zero volts.
- **Output stage:** complementary symmetry push-pull amplifier. It gives low output resistance, large output voltage swing and current sourcing/sinking capability, with short circuit protection.

(Block diagram 2 M, function of blocks 2 M)

Q.3 Attempt any THREE of the following:

12 marks

a) Write ideal and practical values of any four parameters of op-amp.

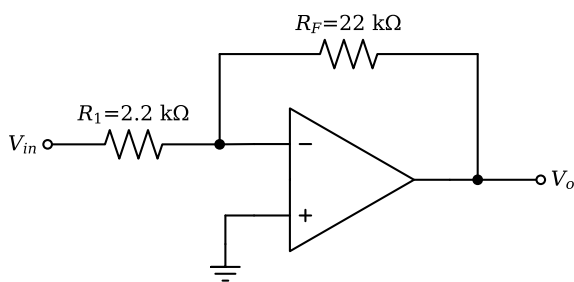
4 M

Parameter	Ideal value	Practical (IC 741, typical)
Input resistance (R_i)	∞	2 M Ω
Output resistance (R_o)	0	75 Ω
Open loop voltage gain (A_{OL})	∞	2×10^5 (106 dB)
CMRR	∞	90 dB
Slew rate (SR)	∞	0.5 V/ μ s
Input offset current (I_{io})	0	20 nA (max 200 nA)

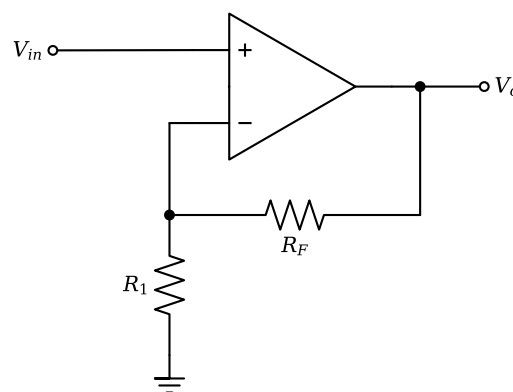
(Any four parameters, 1 M each)

b) If $R_1 = 2.2 \text{ k}\Omega$, $R_F = 22 \text{ k}\Omega$, $V_{CC} = \pm 15 \text{ V}$ and $V_{in} = 0.8 \text{ V rms}$, calculate the output voltage in inverting and non-inverting mode. Draw the circuits.

4 M



(a) Inverting mode



(b) Non-inverting mode

Given: $R_1 = 2.2 \text{ k}\Omega$, $R_F = 22 \text{ k}\Omega$, $V_{in} = 0.8 \text{ V (rms)}$, $V_{CC} = \pm 15 \text{ V}$.

(a) Inverting: $A_V = -R_F/R_1 = -10$; $V_o = -10 \times 0.8 = -8 \text{ V rms}$ (peak = 11.31 V).

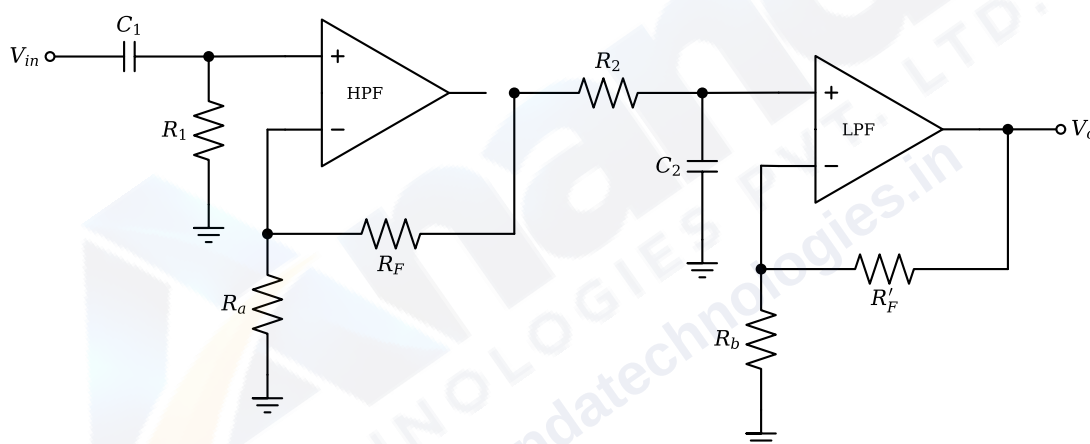
(b) Non-inverting: $A_V = 1 + R_F/R_1 = 11$; $V_o = 11 \times 0.8 = 8.8 \text{ V rms}$ (peak = 12.45 V), in phase with input.

Both peaks are below $V_{sat} \approx 13.5 \text{ V}$, so the outputs are undistorted.

(Circuits 1 M, inverting 1.5 M, non-inverting 1.5 M)

c) Draw and explain the circuit of band pass filter. Draw its frequency response.

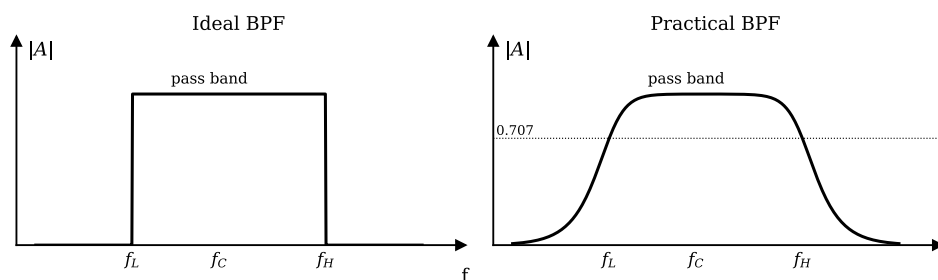
4 M



Wide band pass filter = first order HPF followed by first order LPF

Working (wide band pass filter):

- A first order high pass section (C_1 , R_1) sets the lower cut-off $f_L = 1/(2\pi R_1 C_1)$; it is followed by a first order low pass section (R_2 , C_2) which sets $f_H = 1/(2\pi R_2 C_2)$, with $f_H > f_L$.
- Frequencies below f_L are rejected by the HPF and those above f_H by the LPF, so only the band f_L to f_H is passed.
- Bandwidth $BW = f_H - f_L$; centre frequency $f_C = \sqrt{f_H f_L}$; quality factor $Q = f_C/BW$ (wide band if $Q < 10$). Overall gain = product of the two stage gains.



Frequency response of band pass filter

(Circuit 2 M, explanation 1 M, characteristics 1 M)

d) A class A power amplifier delivers 3 W of AC output power with 25 % efficiency. Calculate the DC power drawn from the supply and the power dissipated. Draw the circuit of class A power amplifier.

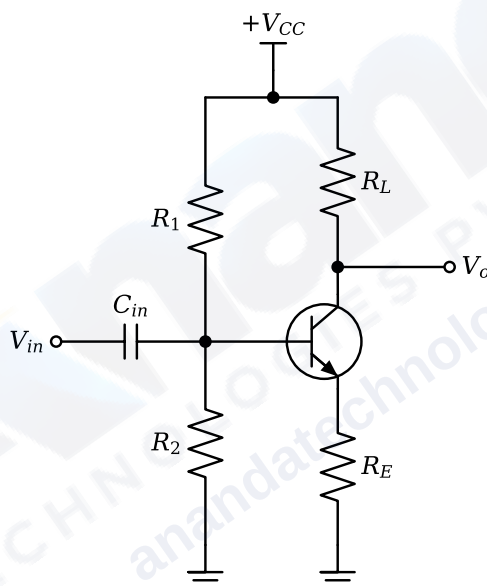
4 M

Given: AC output power $P_{ac} = 3 \text{ W}$, efficiency $\eta = 25 \%$.

Formula: $\eta = P_{ac} / P_{dc} \times 100 \% \Rightarrow P_{dc} = P_{ac} / \eta$

$P_{dc} = 3 / 0.25 = 12 \text{ W}$ (total power drawn from supply)

Power dissipated in the circuit (as heat) = $P_{dc} - P_{ac} = 12 - 3 = 9 \text{ W}$



Single stage directly coupled class A power amplifier

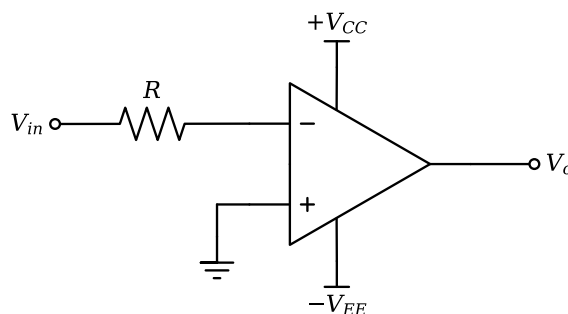
(Calculation 2 M, circuit 2 M)

Q.4 Attempt any THREE of the following:

12 marks

a) Draw and explain inverting zero crossing detector with neat circuit and waveforms.

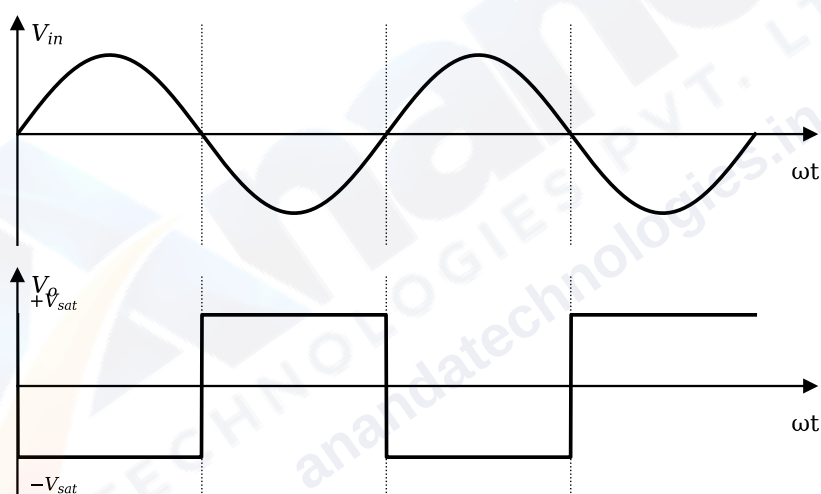
4 M



Inverting zero crossing detector

Working:

- The (+) input is grounded (reference 0 V) and the input is given to the (-) input; the op-amp works in open loop (comparator).
- When V_{in} crosses zero going positive ($V_{in} > 0$), V_{id} is negative $\rightarrow V_o = -V_{sat}$.
- When V_{in} crosses zero going negative ($V_{in} < 0$) $\rightarrow V_o = +V_{sat}$.
- So the output changes state at every zero crossing of input — a sine wave is converted into a square wave (180° out of phase).



Waveforms of inverting zero crossing detector

Applications: sine-to-square conversion, zero-crossing timing marker, phase meter.

(Circuit 1 M, working 2 M, waveforms 1 M)

b) Design an astable multivibrator using IC 555 for frequency 500 Hz and duty cycle 70 %.

Draw the designed circuit. (Assume $C = 0.1 \mu F$)

4 M

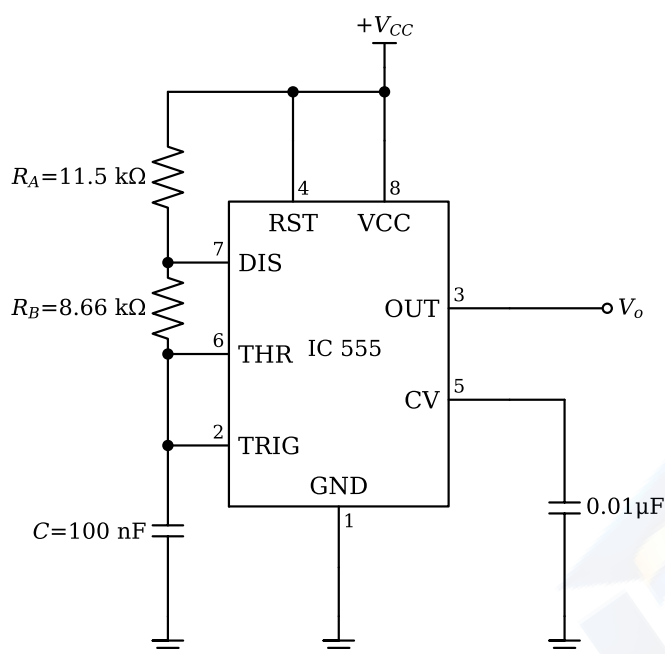
Given: $f = 500 \text{ Hz}$, duty cycle $D = 70 \%$, $C = 100 \text{ nF}$.

$$T = 1/f = 2 \text{ ms}; \quad T_{ON} = D \times T = 1.4 \text{ ms}; \quad T_{OFF} = T - T_{ON} = 600 \mu s$$

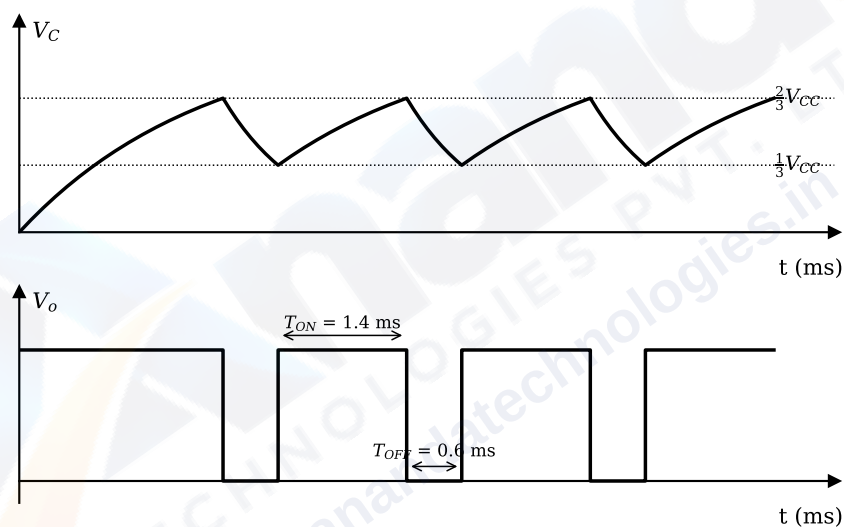
$$T_{OFF} = 0.693 R_B C \Rightarrow R_B = 600 \times 10^{-6} / (0.693 \times 100 \times 10^{-9}) = 8.658 \text{ k}\Omega$$

$$T_{ON} = 0.693(R_A + R_B)C \Rightarrow R_A + R_B = 0.0014 / (0.693 \times 100 \times 10^{-9}) = 20.2 \text{ k}\Omega \Rightarrow R_A = 11.54 \text{ k}\Omega$$

Use standard values / presets: $R_A \approx 12 \text{ k}\Omega$, $R_B \approx 8.2 \text{ k}\Omega$ (fine-tune with presets). Check: $f = 1.44/((R_A + 2R_B)C) = 499 \text{ Hz}$.



Designed astable multivibrator



Capacitor voltage and output waveform of 555 astable multivibrator

(Design 2 M, circuit 2 M)

c) Design RC phase shift oscillator using IC 741 for $f_o = 2 \text{ kHz}$. Draw the designed circuit. (Assume $C = 0.01 \text{ }\mu\text{F}$)

4 M

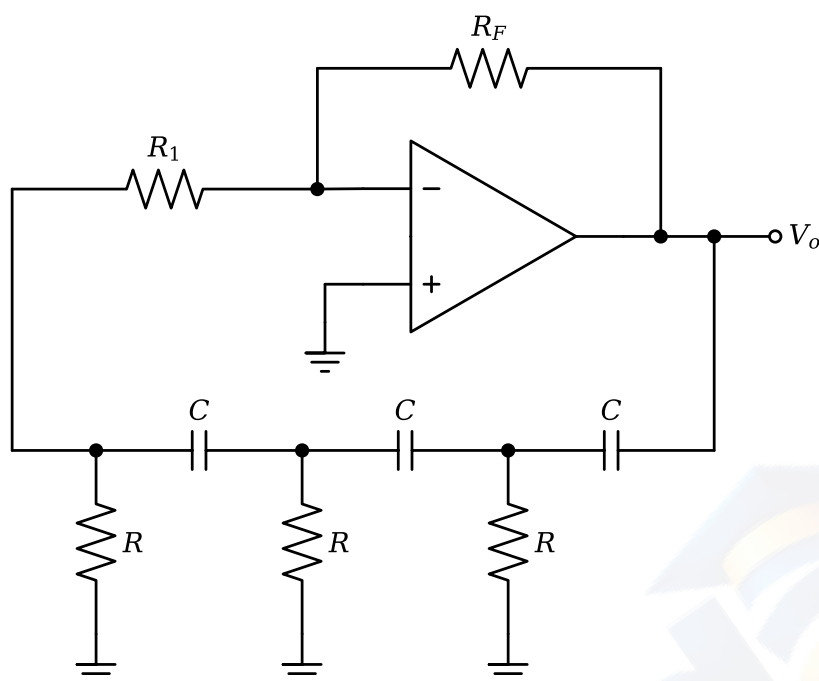
Given: $f_o = 2 \text{ kHz}$. Choose $C = 10 \text{ nF}$.

$$f_o = 1/(2\pi\sqrt{6} RC) \Rightarrow R = 1/(2\pi\sqrt{6} f_o C)$$

$$R = 1 / (2\pi \times 2.449 \times 2000 \times 10 \times 10^{-9}) = \mathbf{3.249 \text{ k}\Omega} \rightarrow \text{use standard } \mathbf{3.3 \text{ k}\Omega} \text{ (gives } f_o = 1.969 \text{ kHz).}$$

To prevent loading: $R_1 = 10R = \mathbf{33 \text{ k}\Omega}$.

For $|A\beta| \geq 1$: $R_F = 29 R_1 = 29 \times 33 \text{ k}\Omega = \mathbf{957 \text{ k}\Omega}$ (use a 1.2 M Ω potentiometer to adjust for clean sine output).



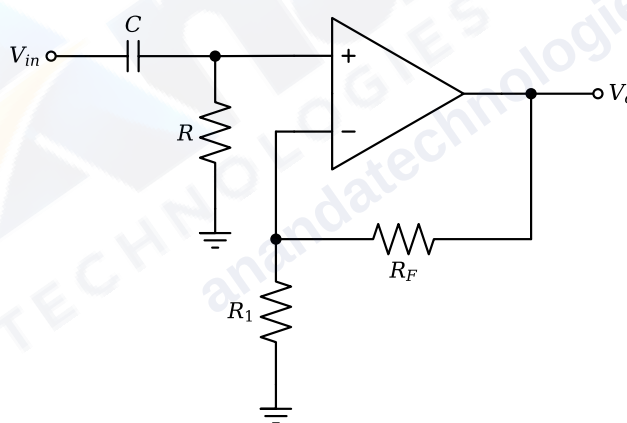
RC feedback network: 3 sections, total phase shift 180°

Designed RC phase shift oscillator: $R = 3.3 \text{ k}\Omega$, $C = 10 \text{ nF}$, $R_1 = 33 \text{ k}\Omega$, $R_F \approx 957 \text{ k}\Omega$

(Design 3 M, circuit 1 M)

d) Draw the circuit diagram of first order high pass filter. Give the expressions for cut-off frequency and pass band gain.

4 M



First order active high pass filter

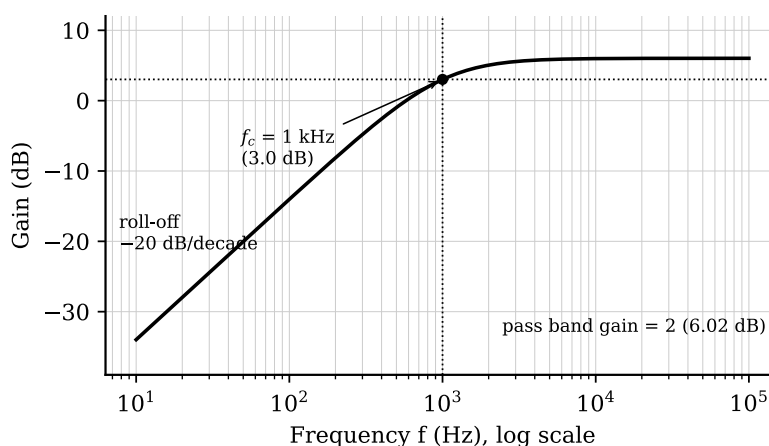
Circuit: A single RC network is connected to the non-inverting input of the op-amp (C in series, R to ground); R_1 and R_F set the pass band gain.

Working / expression: Voltage at (+) input: $V_1 = V_{in} \cdot R / (R + 1/(j2\pi fC)) = V_{in} \cdot 1/(1 - j f_L/f)$

$$V_o/V_{in} = A_F \cdot (j f/f_L)/(1 + j f/f_L)$$

$$f_L = 1/(2\pi RC), \quad \text{pass band gain } A_F = 1 + R_F/R_1$$

For $f < f_L$ the gain is small and rises at 20 dB/decade; for $f > f_L$ the gain $\approx A_F$; at $f = f_L$, gain = $0.707A_F$.

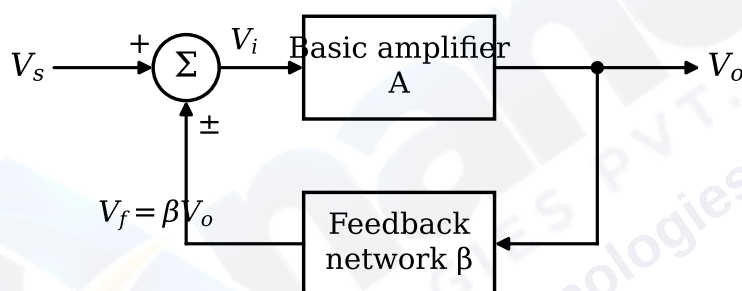


Frequency response of first order high pass filter (example: $f = 1$ kHz, $A_F = 2$)

(Circuit 2 M, expressions 1 M, response 1 M)

e) Draw the block diagram of feedback amplifier and derive the expression for gain with negative feedback.

4 M



$$A_f = A / (1 + A\beta) \text{ for negative feedback}$$

Block diagram of feedback amplifier

Derivation: Let A = gain without feedback, β = feedback factor.

- Output: $V_o = A V_i$
- Feedback voltage: $V_f = \beta V_o$
- For negative feedback: $V_i = V_s - V_f = V_s - \beta V_o$
- $V_o = A(V_s - \beta V_o) \Rightarrow V_o(1 + A\beta) = A V_s$

$$A_f = V_o / V_s = A / (1 + A\beta)$$

$(1 + A\beta)$ is the desensitivity factor; $A\beta$ is the loop gain. For positive feedback $A_f = A / (1 - A\beta)$; when $A\beta = 1$ the circuit oscillates.

(Block diagram 2 M, derivation 2 M)

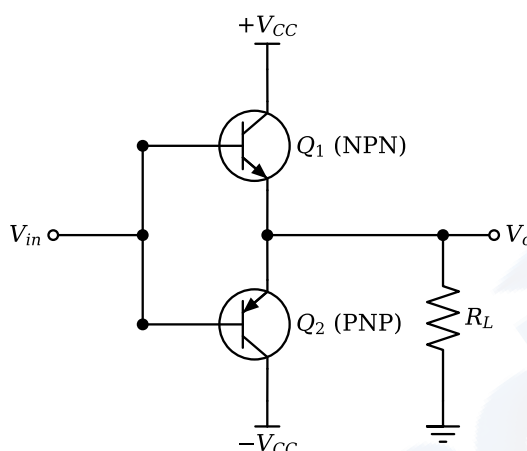
Q.5 Attempt any TWO of the following:

12 marks

a) Draw the class B push-pull amplifier, explain crossover distortion and describe how class AB operation eliminates it, with waveforms.

6 M

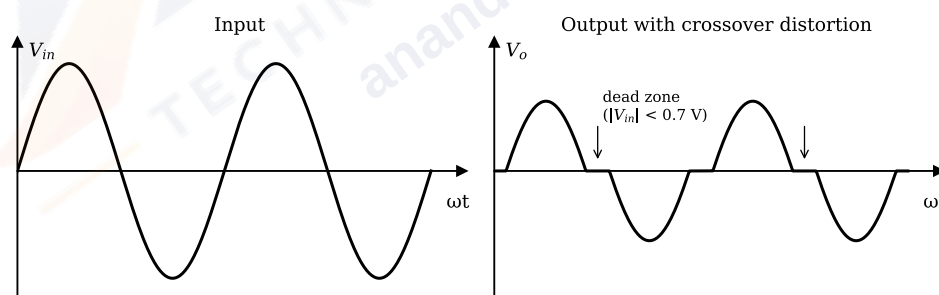
Class B complementary symmetry push-pull amplifier: an NPN transistor Q_1 and a PNP transistor Q_2 with matched characteristics are connected in series with their emitters joined to the load. Both are biased at cut-off. Q_1 amplifies the positive half cycle and Q_2 the negative half cycle; the two halves combine in R_L . No centre-tapped transformer is needed.



Class B complementary symmetry push-pull amplifier

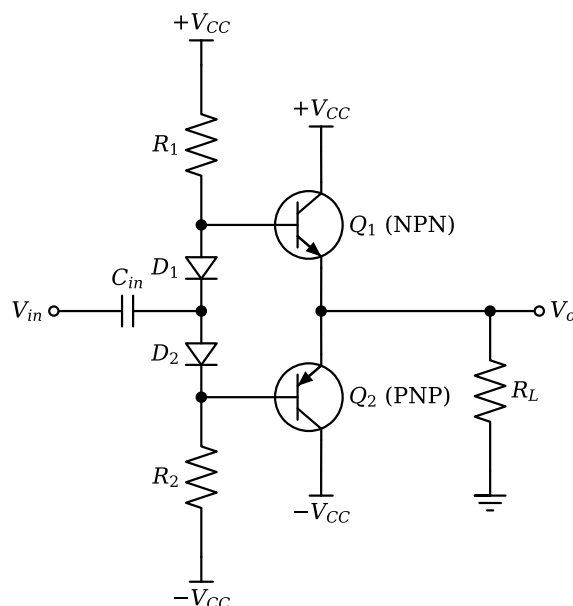
Crossover distortion:

- In class B the transistors have zero bias. A transistor starts conducting only when V_{BE} exceeds the cut-in voltage (≈ 0.7 V for Si).
- So, when the input is between -0.7 V and $+0.7$ V, both transistors are OFF and the output is zero (dead zone).
- The output waveform is therefore distorted near every zero crossing, where the signal "crosses over" from one transistor to the other. This is called crossover distortion.



Crossover distortion in class B push-pull amplifier

Method to overcome: Give a small forward bias (≈ 0.7 V) to each transistor so that both conduct slightly at zero signal — i.e. operate in **class AB**. This bias is given by two diodes D_1 , D_2 (diode biasing, which also gives thermal stability) or by a voltage divider / V_{BE} multiplier.

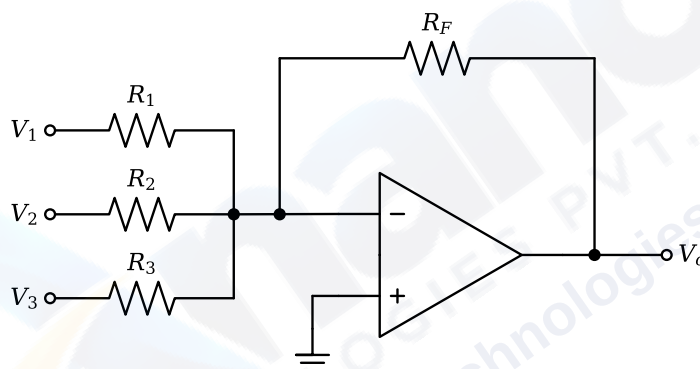


Class AB complementary symmetry push-pull amplifier (diode biasing)

(Class B circuit 1 M, crossover distortion 2 M, waveforms 1 M, class AB remedy 2 M)

b) Draw an inverting summing amplifier with three inputs and derive its output voltage. Calculate V_o if $V_1 = 1$ V, $V_2 = 2$ V, $V_3 = -0.5$ V and all resistors are 10 k Ω .

6 M



Inverting summing amplifier (adder)

Derivation: Point A is at virtual ground and no current enters the op-amp, so the input currents add up in R_F :

$$I_1 + I_2 + I_3 = I_F \Rightarrow V_1/R_1 + V_2/R_2 + V_3/R_3 = -V_o/R_F$$

$$V_o = -R_F (V_1/R_1 + V_2/R_2 + V_3/R_3)$$

If $R_1 = R_2 = R_3 = R_F$: $V_o = -(V_1 + V_2 + V_3)$ (inverting adder).

Calculation: $V_1 = 1$ V, $V_2 = 2$ V, $V_3 = -0.5$ V; $R_1 = 10$ k Ω , $R_2 = 10$ k Ω , $R_3 = 10$ k Ω , $R_F = 10$ k Ω .

$$V_o = -((1) + (2) + (-0.5)) = -2.5 \text{ V}$$

(Circuit 2 M, derivation 2 M, calculation 2 M)

c) Comment on the effect of negative feedback on gain, input resistance and output resistance of amplifiers. Explain the gain-bandwidth product and its importance.

6 M

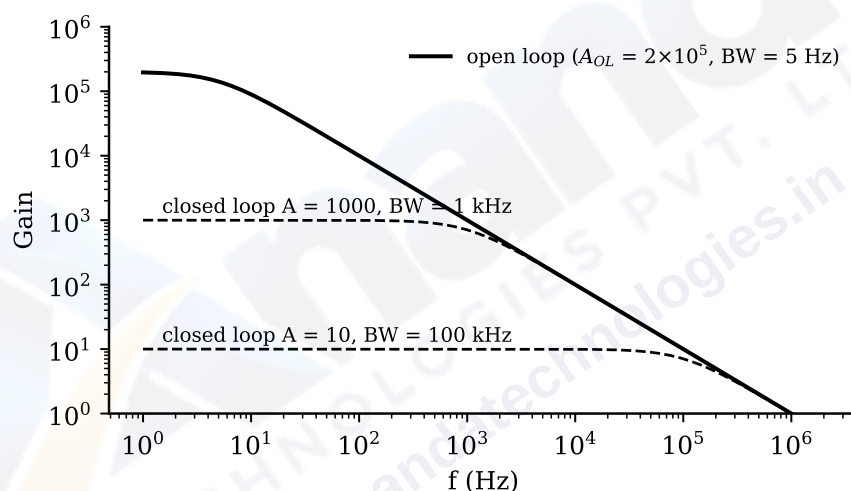
In negative feedback the feedback signal is out of phase with input ($V_i = V_s - \beta V_o$).

- **Gain:** reduces to $A_f = A / (1 + A\beta)$. If $A\beta \gg 1$, $A_f \approx 1/\beta$, i.e. gain depends only on the feedback network, so it becomes stable.
- **Input resistance:** with series mixing (voltage-series / current-series), $R_{if} = R_i(1 + A\beta)$ — increases. With shunt mixing it decreases: $R_{if} = R_i/(1 + A\beta)$.
- **Output resistance:** with voltage sampling, $R_{of} = R_o/(1 + A\beta)$ — decreases (better voltage source). With current sampling it increases.
- **Bandwidth:** increases to $BW_f = BW(1 + A\beta)$; distortion and noise reduce by the factor $(1 + A\beta)$.

Gain–bandwidth product (GBW): For an amplifier with a single dominant pole, the product of gain and bandwidth is constant: $A \times BW = A_f \times BW_f = GBW$ (for IC 741, $GBW \approx 1$ MHz, also called unity-gain bandwidth).

Example (computed): $A_{OL} = 2 \times 10^5$, $BW = 5$ Hz $\Rightarrow$ $GBW = 1$ MHz. With feedback giving $A_f = 10$, $BW_f = GBW/A_f = 100$ kHz.

Importance: GBW tells the designer the maximum bandwidth available for a required closed-loop gain (or the maximum gain for a required bandwidth); it shows that negative feedback trades gain for bandwidth.



Negative feedback: gain reduces, bandwidth increases (gain $\times$ bandwidth = constant)

(Effects on gain, R_i , R_o 3 M; GBW and importance 3 M)

Q.6 Attempt any TWO of the following:

12 marks

a) Design a second order Butterworth high pass filter with lower cut-off frequency 1 kHz.

Draw the designed circuit and its frequency response. (Assume $C = 0.01 \mu F$)

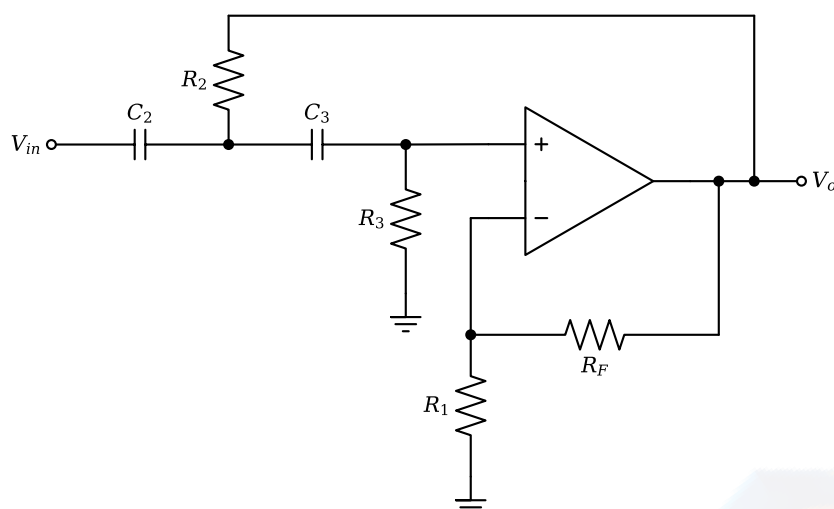
6 M

Given: $f_L = 1$ kHz. For a second order Butterworth response (Sallen-Key, equal components $R_2 = R_3 = R$, $C_2 = C_3 = C$), the pass band gain must be $A_F = 1.586$ (damping 0.707).

Step 1: $f_L = 1/(2\pi RC)$ (equal components). Choose $C = 10$ nF.

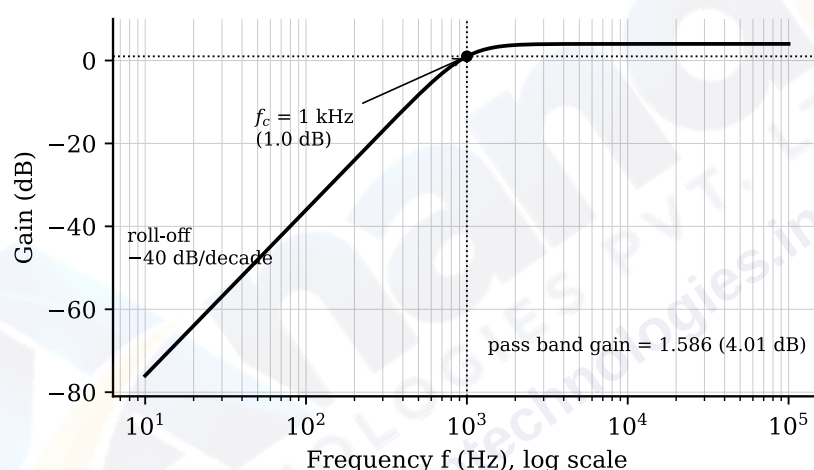
Step 2: $R = 1/(2\pi f_L C) = 1/(2\pi \times 1000 \times 10 \times 10^{-9}) = 15.92 \text{ k}\Omega \rightarrow$ use $15 \text{ k}\Omega$ standard ($f = 1.061$ kHz) or a preset for exact value.

Step 3: $A_F = 1 + R_F/R_1 = 1.586 \Rightarrow R_F = 0.586 R_1$. Choose $R_1 = 10 \text{ k}\Omega \Rightarrow R_F = 5.86 \text{ k}\Omega$ (use $5.6 \text{ k}\Omega + 270 \text{ }\Omega$, or a $10 \text{ k}\Omega$ pot).



Designed second order Butterworth high pass filter

Component values: $R_2 = R_3 = 15 \text{ k}\Omega$, $C_2 = C_3 = 10 \text{ nF}$, $R_1 = 10 \text{ k}\Omega$, $R_F = 5.86 \text{ k}\Omega$, op-amp IC 741 with $\pm 15 \text{ V}$ supply.

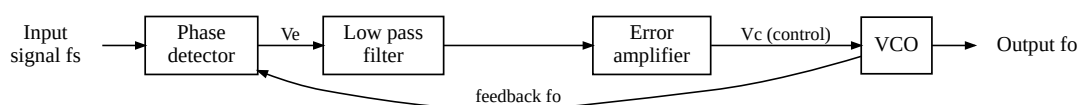


Actual frequency response: gain 1.586 (4.0 dB) in pass band, -3 dB at 1 kHz, roll-off 40 dB/decade

(Design 3 M, circuit 2 M, frequency response 1 M)

b) Draw the block diagram of PLL and explain its operation. Define lock range and capture range.

6 M



Block diagram of phase locked loop (PLL)

- **Phase detector:** compares the phase/frequency of input signal f_s with the VCO output f_o and produces a DC (error) voltage V_e proportional to the phase difference.
- **Low pass filter:** removes the high frequency components and noise from the phase detector output and passes the DC/slowly varying error voltage; it also controls capture range and transient response.

- **Error amplifier:** amplifies the filtered error voltage to give the control voltage V_c .
- **VCO:** its output frequency changes in proportion to V_c , in the direction that reduces the frequency difference until $f_o = f_s$ (locked).

Operation: When there is no input, the VCO runs at its free running frequency f_o . When an input is applied, the loop pulls the VCO frequency towards f_s ; when $f_o = f_s$ the loop is in **lock** and it then tracks changes of input frequency.

Lock range (tracking range): the range of input frequencies over which the PLL, once locked, remains in lock (tracks the input). It is expressed as $\pm \Delta f_L$ about the free running frequency.

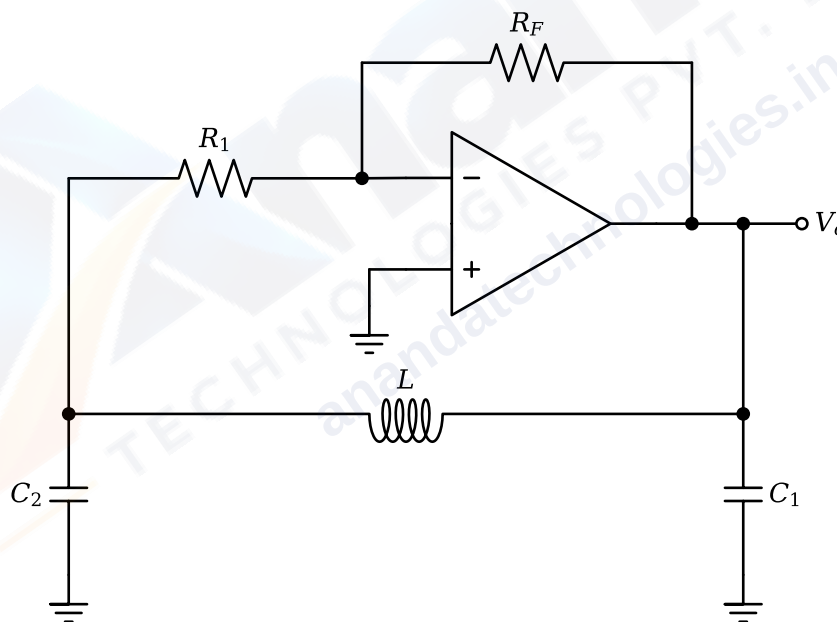
Capture range (acquisition range): the range of input frequencies over which the PLL can acquire (establish) lock starting from the unlocked condition. Capture range is always smaller than (or equal to) the lock range.

(Block diagram 2 M, functions 2 M, lock / capture range 2 M)

c) Explain Colpitts oscillator using op-amp and derive its frequency of oscillation. Calculate f_o for $L = 1 \text{ mH}$, $C_1 = 0.01 \text{ }\mu\text{F}$ and $C_2 = 0.1 \text{ }\mu\text{F}$.

6 M

Circuit: The op-amp is an inverting amplifier (180° phase shift, gain $-R_F/R_1$). The tank circuit consists of two capacitors C_1 , C_2 (tapped capacitor) and one inductor L . Element 1 is across the output, element 2 across the amplifier input side and element 3 between them; the tank gives another 180° , so total phase shift is 360° .



Colpitts oscillator using op-amp

Working: At switch ON, noise starts oscillation in the tank circuit. The voltage across element 2 is fed back to the amplifier input through R_1 ; the amplifier supplies the energy lost in the tank so that the oscillations are sustained at the resonant frequency of the tank.

Derivation of frequency (general LC oscillator, amplifier output resistance R_o):

Let $X_1 = -1/(\omega C_1)$, $X_2 = -1/(\omega C_2)$, $X_3 = \omega L$. The loop gain of the general LC oscillator is

$$A\beta = -A X_1 X_2 / [jR_o(X_1 + X_2 + X_3) - X_1(X_2 + X_3)]$$

For $A\beta$ to be a real number (phase condition) the imaginary term must be zero:

$$X_1 + X_2 + X_3 = 0$$

$$-1/(\omega C_1) - 1/(\omega C_2) + \omega L = 0 \Rightarrow \omega^2 = (C_1 + C_2)/(L C_1 C_2)$$

$$f_o = 1 / (2\pi \sqrt{L C_{eq}}), \quad C_{eq} = C_1 C_2 / (C_1 + C_2)$$

Using $X_2 + X_3 = -X_1$, the magnitude condition $|A\beta| = 1$ gives $|A| = X_1/X_2 = C_2/C_1 \Rightarrow R_F/R_1 \geq C_2/C_1$.

Calculation: $L = 1 \text{ mH}$, $C_1 = 10 \text{ nF}$, $C_2 = 100 \text{ nF}$

$$C_{eq} = C_1 C_2 / (C_1 + C_2) = 9.091 \text{ nF}$$

$$f_o = 1/(2\pi \sqrt{L C_{eq}}) = 1/(2\pi \sqrt{0.001 \times 9.091 \times 10^{-9}}) = \mathbf{52.79 \text{ kHz}}$$

Minimum gain $|A| = C_2/C_1 = \mathbf{10} \Rightarrow$ choose $R_1 = 10 \text{ k}\Omega$, $R_F \geq 100 \text{ k}\Omega$.

(Circuit 2 M, working 1 M, derivation 3 M)

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