Analog Electronics (313324)

MSBTE K-Scheme · Model Question Paper — Set A · Model Answers

Q.1 Attempt any FIVE of the following: 10 marks

a) Classify power amplifiers on the basis of conduction angle and coupling. 2 M

Classification of power amplifiers:

- **Based on conduction angle (Q-point):** Class A (360°), Class B (180°), Class AB (between 180° and 360°), Class C (less than 180°). (Class D – switching type.)
- **Based on coupling:** RC (capacitor) coupled, transformer coupled, direct coupled.
- **Based on configuration:** single-ended, push-pull, complementary symmetry push-pull.
- **Based on frequency:** audio frequency (AF) and radio frequency (RF / tuned) power amplifiers.

(Any two correct bases with types, 1 M each)

b) State the Barkhausen criteria for sustained oscillations. 2 M

For sustained oscillations, the following two conditions (Barkhausen criteria) must be satisfied:

1. The magnitude of loop gain must be unity: $|A\beta| = 1$.
2. The total phase shift around the loop must be **0° or 360°** (i.e. feedback must be positive).

(Each condition 1 M)

c) Define the following parameters of op-amp and write their typical values for IC 741: i) Slew rate ii) CMRR 2 M

Slew rate (SR): The maximum rate of change of output voltage per unit time: SR = $(dV_o/dt)_{max}$, expressed in V/µs. Ideal value: ∞; typical for IC 741: **0.5 V/µs**.

CMRR: Common mode rejection ratio is the ratio of differential mode gain to common mode gain: CMRR = A_d/A_c (in dB: 20 log A_d/A_c). It shows the ability to reject common (noise) signals. Ideal value: ∞; typical for IC 741: **90 dB**.

(Each definition with values 1 M)

d) State the function of the level shifting stage in an op-amp. 2 M

Function of level shifting stage: The input and intermediate stages are direct coupled differential amplifiers, so the DC level at the output of the intermediate stage rises well above ground. The level shifting stage (usually an emitter follower with constant current source) **brings this DC level down to zero volts with respect to ground**, so that the output is zero when the input is zero, without affecting the AC signal.

(Correct function 2 M)

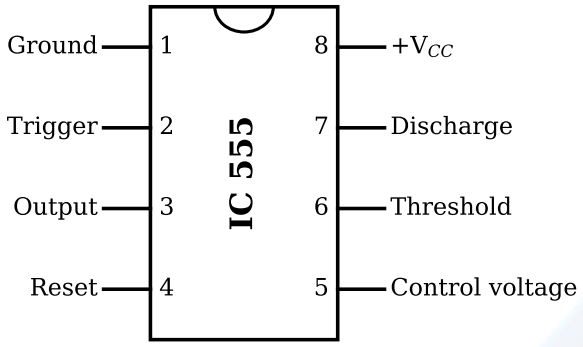
e) Define the following terms related to filters: i) Pass band ii) Roll-off rate 2 M

Pass band: The range of frequencies which the filter passes with (nearly) constant gain, i.e. without attenuation.

Roll-off rate: The rate at which the gain falls in the stop band beyond the cut-off frequency; = 20 dB/decade (6 dB/octave) for each order of the filter.

(Each definition 1 M)

f) Draw the labelled pin diagram of IC 555. 2 M



Pin diagram of IC 555 timer (8-pin DIP, top view)

(Labelled pin diagram 2 M)

g) Define lock range and capture range of a PLL. 2 M

Lock range (tracking range): the range of input frequencies over which the PLL, once locked, remains in lock (tracks the input). It is expressed as $\pm\Delta f_L$ about the free running frequency.

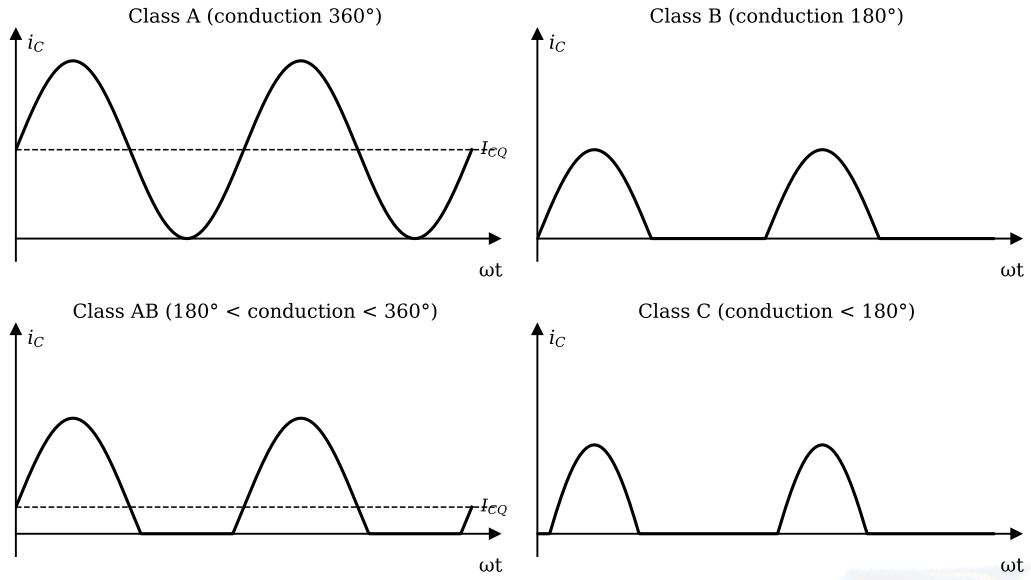
Capture range (acquisition range): the range of input frequencies over which the PLL can acquire (establish) lock starting from the unlocked condition. Capture range is always smaller than (or equal to) the lock range.

(Each definition 1 M)

Q.2 Attempt any THREE of the following: 12 marks

a) Compare class A, class B, class AB and class C power amplifiers on the basis of: i) Conduction angle ii) Position of Q-point iii) Efficiency iv) Distortion 4 M

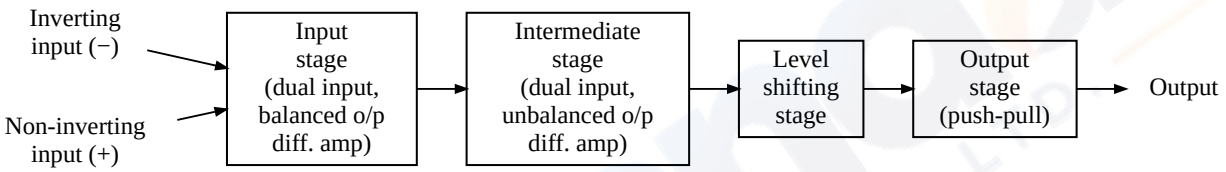
Parameter	Class A	Class B	Class AB	Class C
Conduction angle	360°	180°	Between 180° and 360°	Less than 180°
Position of Q-point	Centre of DC load line	At cut-off (on X-axis)	Slightly above cut-off	Below cut-off (beyond X-axis)
Maximum efficiency	25 % (resistive load), 50 % (transformer coupled)	78.5 %	Between 50 % and 78.5 %	More than 78.5 % (up to ≈ 95 %)
Distortion	Minimum (no distortion)	Crossover distortion	Very small (crossover removed)	Maximum (output current is pulses)



Collector current waveforms of class A, B, AB and C amplifiers

(Each correct parameter 1 M)

b) Draw the block diagram of an op-amp and state the function of each block. 4 M



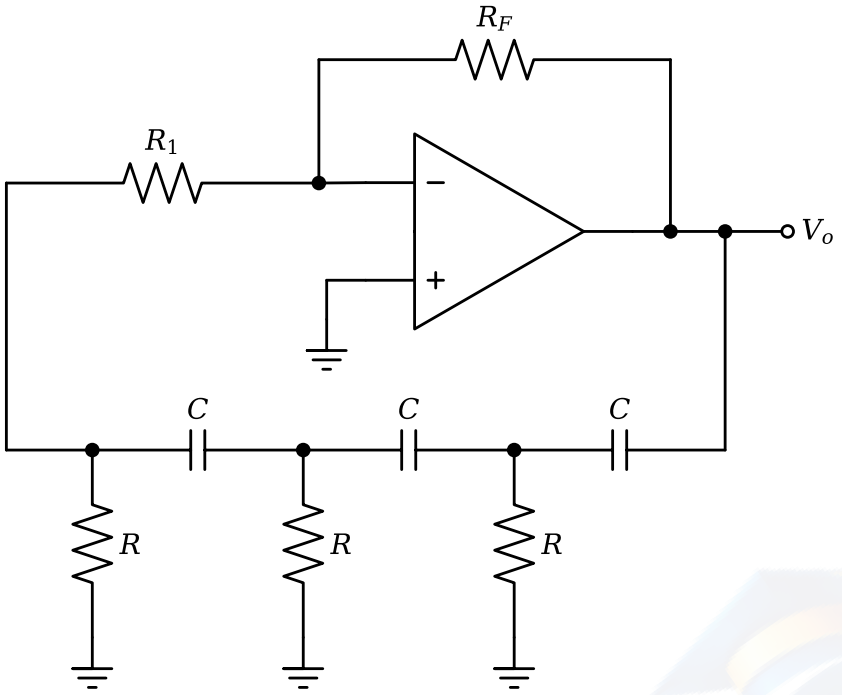
Block diagram of op-amp

- **Input stage:** dual input, balanced output differential amplifier. It provides most of the voltage gain and decides the input resistance (high R_i) and CMRR.
- **Intermediate stage:** dual input, unbalanced (single-ended) output differential amplifier, driven by the input stage. It gives additional voltage gain.
- **Level shifting stage:** emitter follower / constant current source circuit which shifts the DC level at the output of the intermediate stage down to zero volts.
- **Output stage:** complementary symmetry push-pull amplifier. It gives low output resistance, large output voltage swing and current sourcing/sinking capability, with short circuit protection.

(Block diagram 2 M, function of blocks 2 M)

c) Draw the circuit of RC phase shift oscillator using op-amp and explain its working. Write the formula for frequency of oscillation. 4 M

Circuit: The op-amp is used as an inverting amplifier (gain $-R_F/R_1$) which gives 180° phase shift. The feedback network has three identical RC sections, each giving 60°, so total phase shift is 180° + 180° = 360°.



RC feedback network: 3 sections, total phase shift 180°

RC phase shift oscillator using op-amp

Working:

- When power is switched ON, noise voltage appears at the output; it is fed back through the RC network.
- At only one frequency f_o the RC network gives exactly 180° phase shift and attenuation $\beta = 1/29$.
- The amplifier gain is made $|A| = R_F/R_1 \geq 29$, so that $|A\beta| \geq 1$ and the Barkhausen criteria are satisfied — a sustained sine wave of frequency f_o is produced.

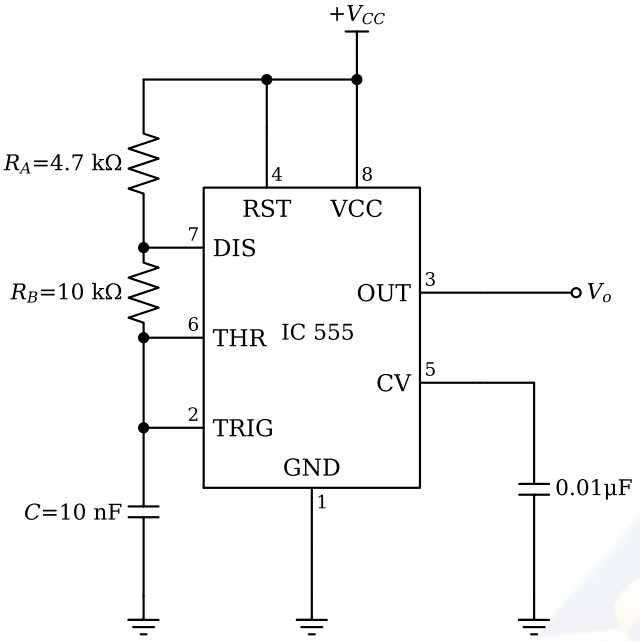
$$\mathbf{f_o = 1 / (2\pi \sqrt{6}\, RC) \quad and \quad R_F = 29\, R_1}$$

To avoid loading of the RC network by the amplifier, $R_1 \geq 10R$.

(Circuit 2 M, working 1 M, formula 1 M)

d) IC 555 is used as an astable multivibrator with R_A = 4.7 kΩ, R_B = 10 kΩ and C = 0.01 µF.

Calculate the frequency of oscillation and duty cycle. Draw the output waveform. 4 M



Astable multivibrator using IC 555

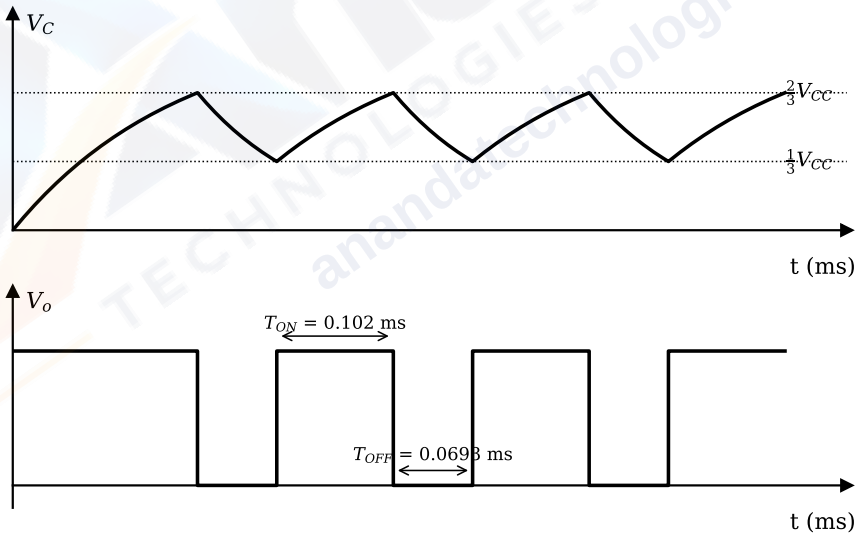
Given: $R_A = R_1 = 4.7\ k\Omega$, $R_B = R_2 = 10\ k\Omega$, $C = 10\ nF$.

$T_{ON} = 0.693(R_A + R_B)C = 0.693 \times 14700 \times 10 \times 10^{-9} =$ **101.9 μs**

$T_{OFF} = 0.693\ R_B C = 0.693 \times 10000 \times 10 \times 10^{-9} =$ **69.3 μs**

$T = T_{ON} + T_{OFF} = 171.2\ \mu s \Rightarrow$ **f = 1/T = 5.842 kHz** (check: $1.44/((R_A + 2R_B)C) = 5.83$ kHz)

Duty cycle $D = (R_A + R_B)/(R_A + 2R_B) \times 100 =$ **59.51 %**



Capacitor voltage and output waveform of 555 astable multivibrator

(Frequency 1.5 M, duty cycle 1.5 M, waveform 1 M)

Q.3 Attempt any THREE of the following: 12 marks

a) State the advantages and disadvantages of negative feedback in amplifiers. 4 M

Advantages of negative feedback:

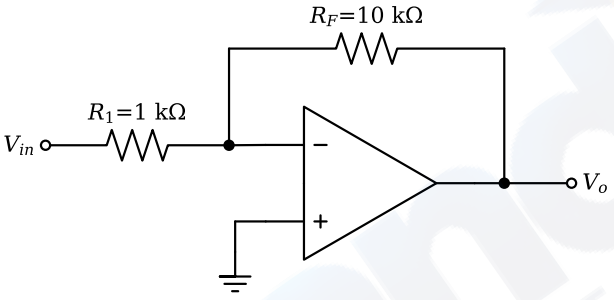
- Gain becomes stable (less dependent on transistor parameters, temperature, supply).
- Bandwidth increases (gain × bandwidth remains constant).
- Non-linear distortion and noise are reduced.
- Input resistance increases (series mixing) and output resistance decreases (voltage sampling) — useful for impedance matching.
- Frequency response becomes flat and operation is more linear.

Disadvantages:

- Overall gain is reduced ($A_f = A/(1 + A\beta)$), so more stages are needed for the same gain.
- Circuit becomes more complex; at high frequencies extra phase shift may make it unstable (oscillate).

(Advantages 2 M, disadvantages 2 M)

b) In an inverting amplifier R_1 = 1 kΩ, R_F = 10 kΩ and V_{in} = 0.5 V (peak) sine wave at 1 kHz. Calculate the output voltage and sketch the input and output waveforms. 4 M



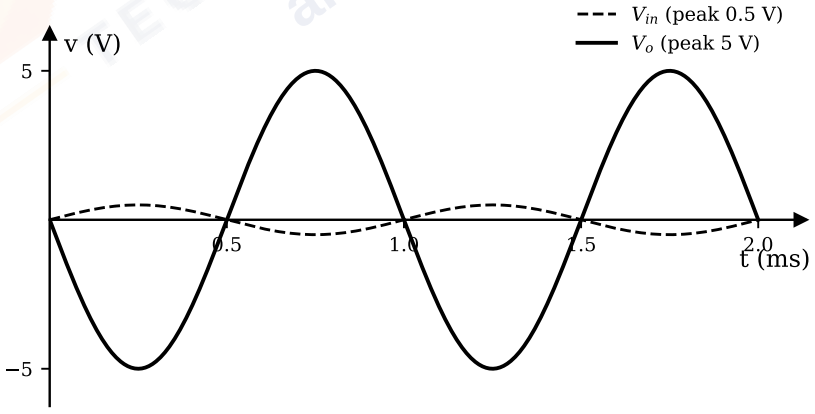
Closed loop inverting amplifier

Given: R_1 = 1 kΩ, R_F = 10 kΩ, V_{in} = 0.5 V peak sine wave at 1 kHz.

Closed loop gain $A_V = -R_F/R_1 = -10000/1000 =$ **−10**

$V_o = A_V \times V_{in} = -10 \times 0.5 =$ **−5 V peak** (5 V peak sine wave, 180° out of phase with input, frequency 1 kHz).

Since 5 V < V_{sat} (≈ ±13.5 V for ±15 V supply), the output is not clipped.



Input and output waveforms (output is 180° out of phase)

(Gain 1 M, output 1 M, waveforms 2 M)

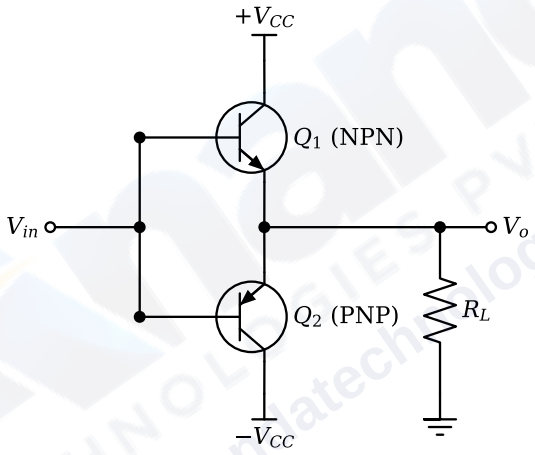
c) Compare active filters and passive filters. (Any four points) 4 M

Active filter	Passive filter
Uses active elements (op-amp / transistor) along with R and C.	Uses only passive elements R, L, C.
Can provide gain (pass band gain ≥ 1).	Gain is always less than 1 (insertion loss).
Inductors are not needed, so small size, light weight and low cost at low frequencies.	Inductors are bulky, heavy and costly at low frequencies.
High input and low output impedance — no loading problem; easy cascading.	Loading effect is present; cascading changes the response.

(Any 4 points, 1 M each)

d) Draw the circuit of class B complementary symmetry push-pull amplifier. Explain crossover distortion with waveforms. 4 M

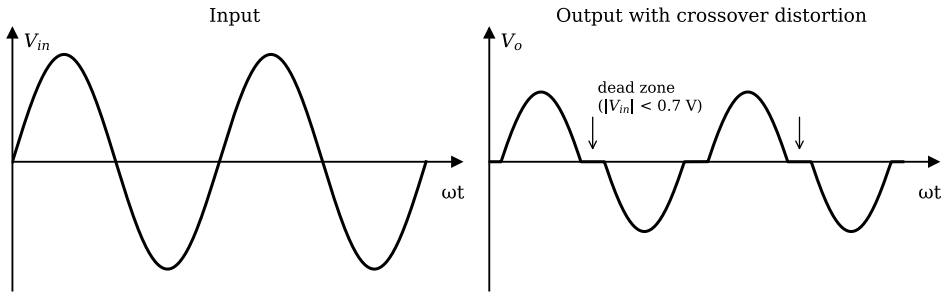
Class B complementary symmetry push-pull amplifier: an NPN transistor Q_1 and a PNP transistor Q_2 with matched characteristics are connected in series with their emitters joined to the load. Both are biased at cut-off. Q_1 amplifies the positive half cycle and Q_2 the negative half cycle; the two halves combine in R_L. No centre-tapped transformer is needed.



Class B complementary symmetry push-pull amplifier

Crossover distortion:

- In class B the transistors have zero bias. A transistor starts conducting only when V_{BE} exceeds the cut-in voltage (≈ 0.7 V for Si).
- So, when the input is between −0.7 V and +0.7 V, both transistors are OFF and the output is zero (dead zone).
- The output waveform is therefore distorted near every zero crossing, where the signal "crosses over" from one transistor to the other. This is called crossover distortion.

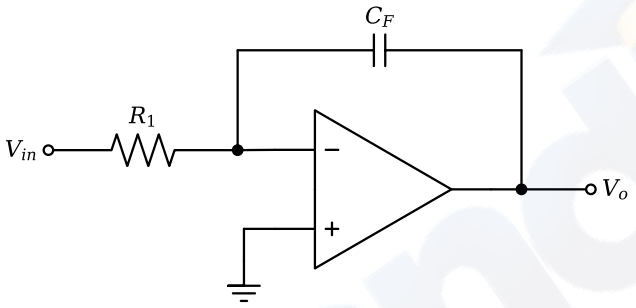


Crossover distortion in class B push-pull amplifier

(Circuit 2 M, crossover distortion with waveform 2 M)

Q.4 Attempt any THREE of the following: 12 marks

a) Draw the circuit of an op-amp integrator. Derive the expression for its output voltage and draw input-output waveforms. 4 M



Basic op-amp integrator

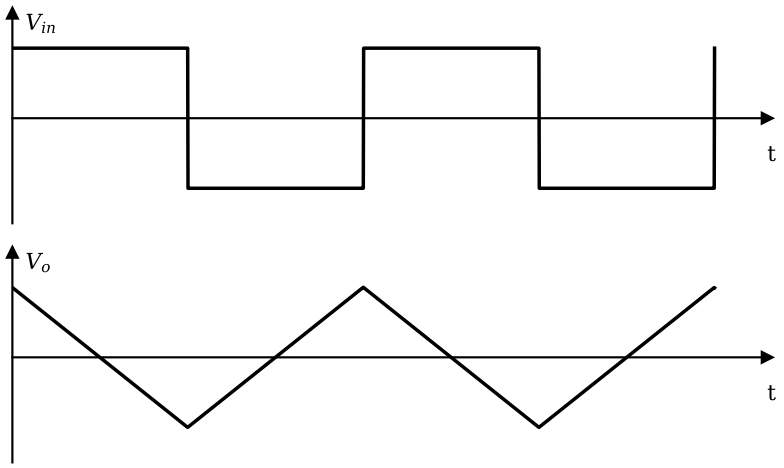
Derivation: Point A is at virtual ground ($V_A = 0$) and the op-amp input current is zero, so the current through R_1 flows through C_F:

$$\mathbf{i = V_{in}/R_1 = C_F\, d(V_A - V_o)/dt = -C_F\, dV_o/dt}$$

Integrating both sides with respect to time:

$$\mathbf{V_o = -(1/R_1C_F) \int_0^t V_{in}\, dt + V_o(0)}$$

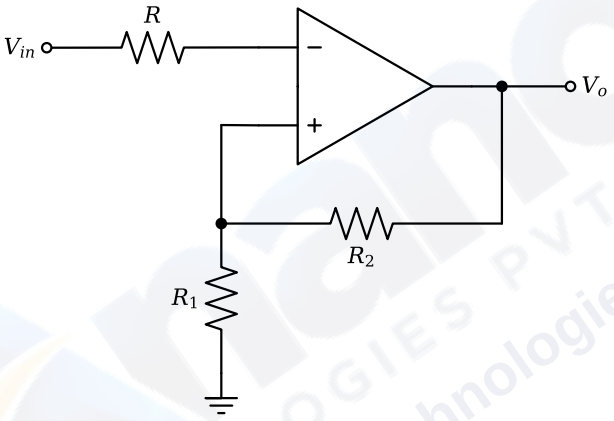
So the output is proportional to the time integral of input (with sign inversion). For a square wave input the output is a triangular wave. (In practice a resistor R_F is connected across C_F to limit low-frequency gain — practical integrator.)



Integrator: square wave input gives triangular output

(Circuit 1 M, derivation 2 M, waveforms 1 M)

b) In an inverting Schmitt trigger, R_1 = 1 kΩ (from non-inverting input to ground), R_2 = 47 kΩ (from output to non-inverting input), V_{sat} = ±13.5 V and V_{in} = 1 $V_{p\text{-}p}$ sine wave. Calculate V_{UT}, V_{LT} and hysteresis voltage V_H. 4 M



Inverting Schmitt trigger: R1 from (+) input to ground, R2 from output to (+) input

Working: Positive feedback through R_2–R_1 gives a reference $V_{ref} = R_1 V_o/(R_1 + R_2)$ at the (+) input. When $V_o = +V_{sat}$ the input must rise above V_{UT} to switch the output to $-V_{sat}$; it then switches back only when the input falls below V_{LT}.

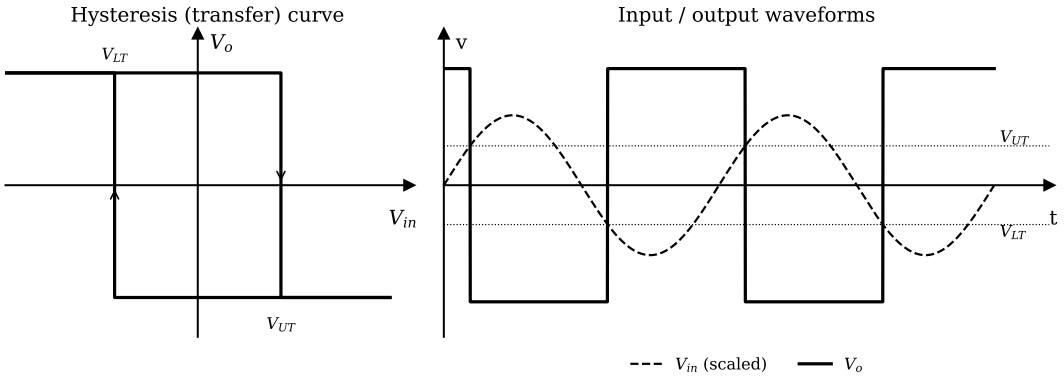
Given: R_1 = 1 kΩ, R_2 = 47 kΩ, V_{sat} = ±13.5 V, V_{in} = 1 $V_{p\text{-}p}$ (peak 0.5 V).

(i) $V_{UT} = R_1(+V_{sat})/(R_1 + R_2) = 1000 \times 13.5 / (1000 + 47000)$ = **281.2 mV**

(ii) $V_{LT} = R_1(-V_{sat})/(R_1 + R_2)$ = **-281.2 mV**

(iii) Hysteresis $V_H = V_{UT} - V_{LT} = 2R_1V_{sat}/(R_1 + R_2)$ = **562.5 mV**

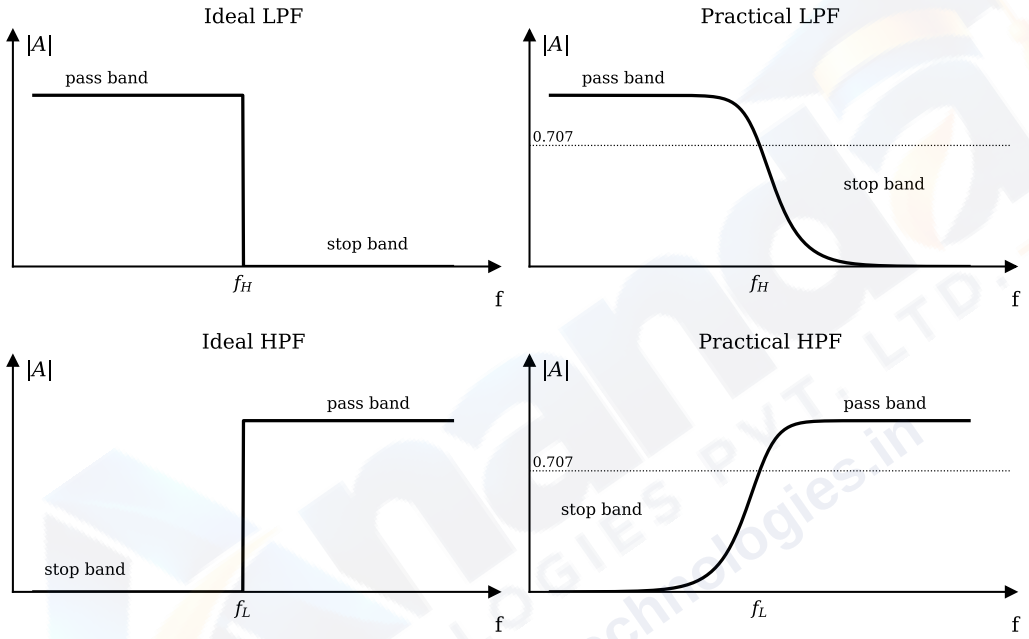
Since the input peak (0.5 V) is larger than V_{UT}, the output switches every cycle and a square wave is obtained.



Schmitt trigger characteristics

(Circuit 1 M, each value 1 M)

c) Draw the ideal and practical frequency response of: i) Low pass filter ii) High pass filter 4 M

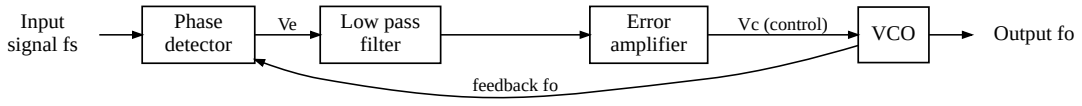


Ideal and practical frequency response

An ideal filter has constant gain in the pass band and zero gain in the stop band with a vertical transition at f_c. A practical filter has a gradual transition; at f_c the gain is 0.707 (−3 dB) of the pass band gain and then falls at the roll-off rate.

(Each graph 1 M)

d) Draw the block diagram of PLL and state the function of each block. 4 M



Block diagram of phase locked loop (PLL)

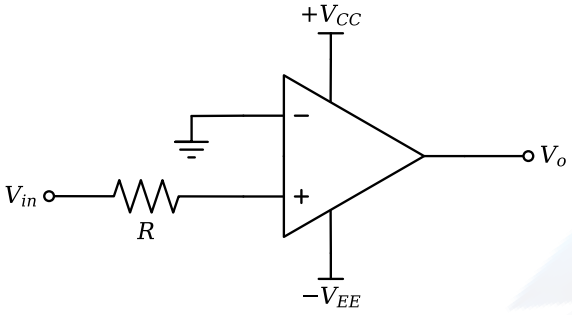
- **Phase detector:** compares the phase/frequency of input signal f_s with the VCO output f_o and produces a DC (error) voltage V_e proportional to the phase difference.
- **Low pass filter:** removes the high frequency components and noise from the phase detector output and passes the DC/slowly varying error voltage; it also controls capture range and

transient response.

- **Error amplifier:** amplifies the filtered error voltage to give the control voltage V_c.
- **VCO:** its output frequency changes in proportion to V_c, in the direction that reduces the frequency difference until $f_o = f_s$ (locked).

(Block diagram 2 M, functions 2 M)

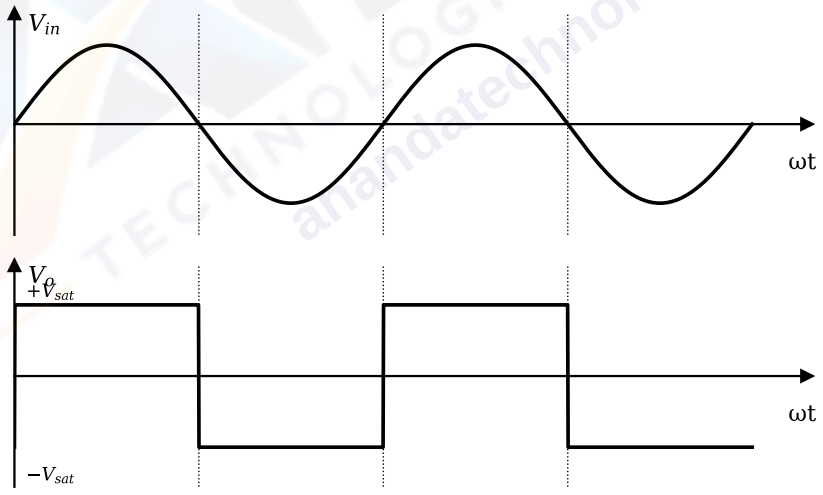
e) Describe the working of a non-inverting zero crossing detector with circuit diagram and waveforms. 4 M



Non-inverting zero crossing detector

Working:

- The (−) input is grounded (reference 0 V) and the input is given to the (+) input; the op-amp works in open loop (comparator).
- When $V_{in} > 0$ (positive half cycle), V_{id} is positive → $V_o = +V_{sat}$.
- When $V_{in} < 0$ (negative half cycle) → $V_o = -V_{sat}$.
- The output changes state each time the input crosses zero — sine to square wave conversion (in phase with input).



Waveforms of non-inverting zero crossing detector

Applications: sine-to-square conversion, zero-crossing timing marker, phase meter.

(Circuit 1 M, working 2 M, waveforms 1 M)

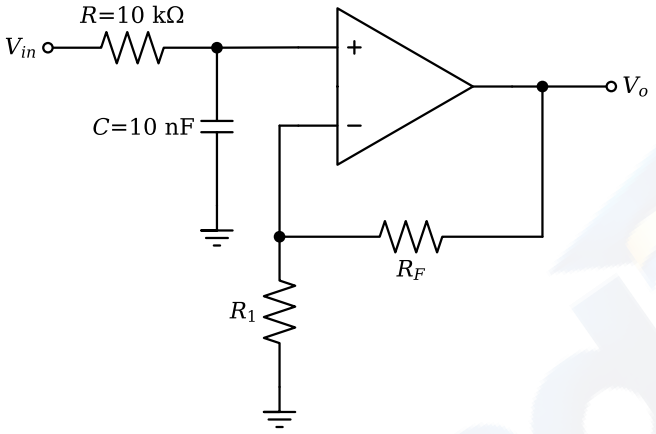
Q.5 Attempt any TWO of the following: 12 marks

a) Design a first order active low pass filter with cut-off frequency 1.5 kHz and pass band gain 2. Draw the designed circuit and its frequency response. (Assume C = 0.01 µF) 6 M

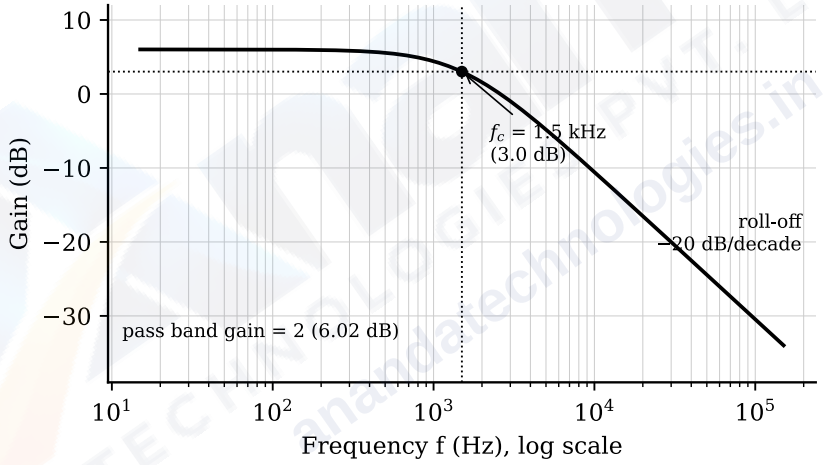
Given: f_H = 1.5 kHz, pass band gain A_F = 2. **Step 1:** choose C = 10 nF.

Step 2: R = 1/(2πf C) = 1/(2π × 1500 × 10 × 10^{-9}) = **10.61 kΩ** → use standard 10 kΩ (actual f = 1.592 kHz), or a 10.6 kΩ preset for exact value.

Step 3: $A_F = 1 + R_F/R_1 = 2 \Rightarrow R_F = 1\ R_1$. Choose R_1 = 10 kΩ ⇒ R_F = **10 kΩ**.



Designed first order low pass filter (R1 = 10 kΩ, RF = 10 kΩ)

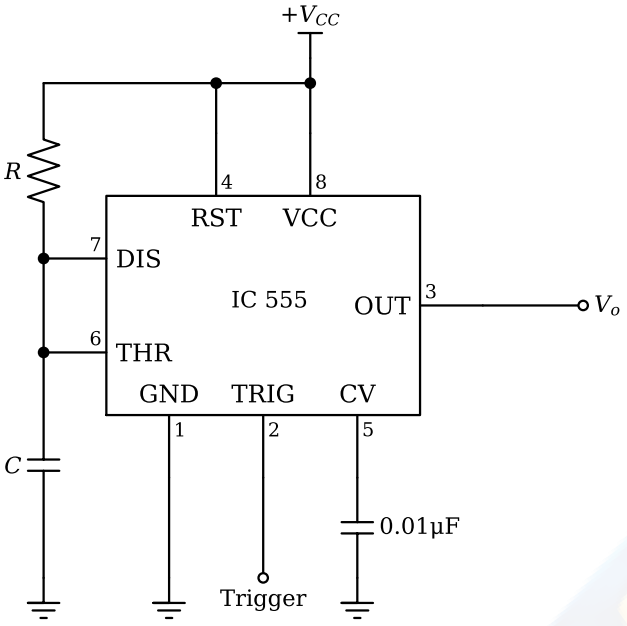


Frequency response of designed first order LPF

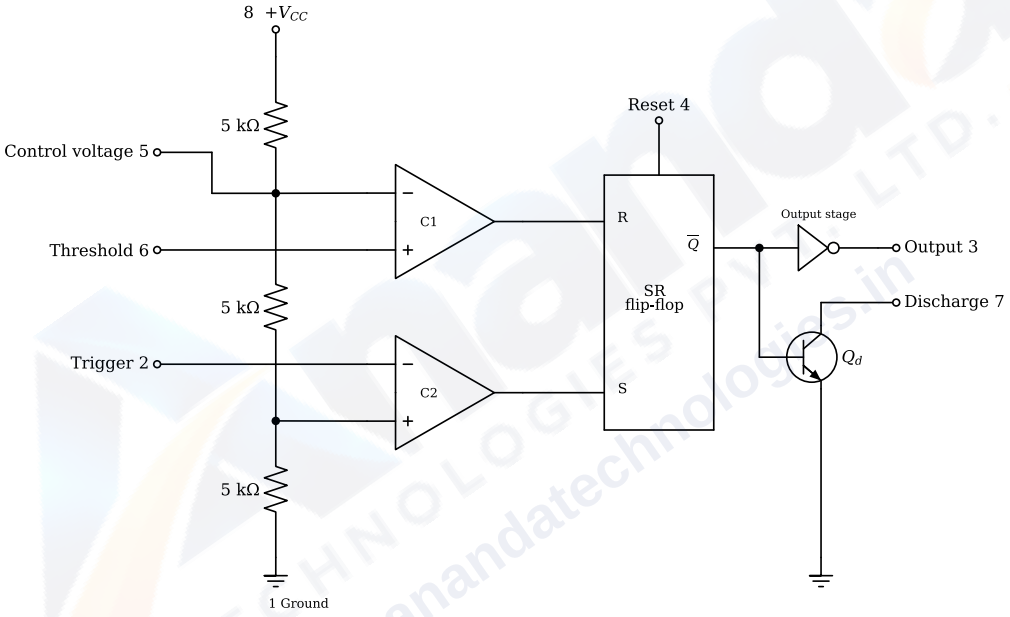
(Design 3 M, circuit 2 M, response 1 M)

b) Draw the circuit of monostable multivibrator using IC 555 and explain its working with the help of internal block diagram and waveforms. Calculate the pulse width for R = 47 kΩ

and C = 10 µF. 6 M



Monostable multivibrator using IC 555



Functional (internal) block diagram of IC 555

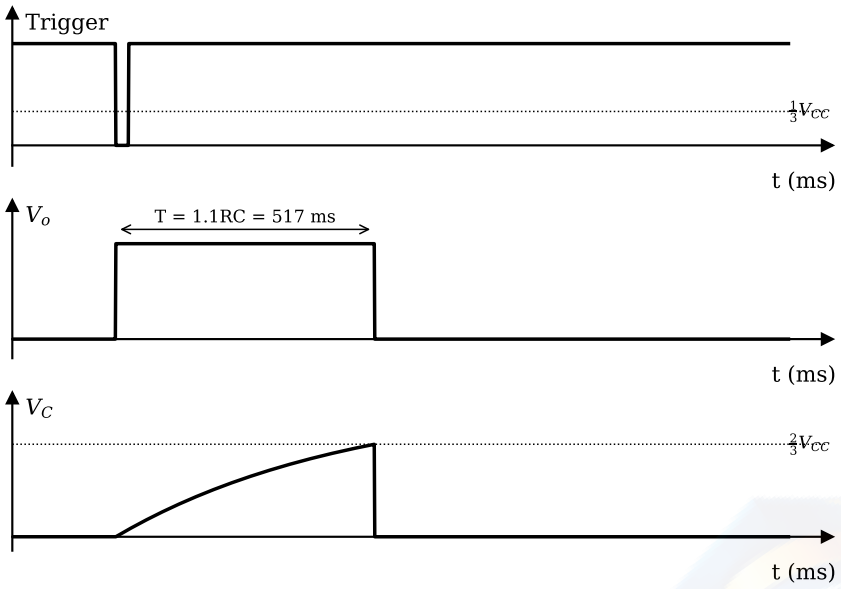
Working:

- **Stable state:** output LOW; the flip-flop is reset, discharge transistor is ON and holds the capacitor at 0 V.
- When a negative trigger pulse (below $V_{CC}/3$) is applied at pin 2, the lower comparator sets the flip-flop: output goes HIGH and the discharge transistor turns OFF (quasi-stable state).
- C charges through R towards V_{CC}. When V_C reaches $2V_{CC}/3$ the upper comparator resets the flip-flop: output returns LOW, the transistor turns ON and C discharges quickly.
- The circuit stays in the stable state till the next trigger. Pulse width:

$$\mathbf{T = 1.1\ RC}$$

(From $V_C = V_{CC}(1 - e^{-t/RC}) = 2V_{CC}/3 \Rightarrow t = RC \ln 3 = 1.0986\ RC \approx 1.1RC$.)

Example (computed): R = 47 kΩ, C = 10 µF ⇒ T = 1.1 × 47000 × 10 × 10^{-6} = **517 ms**

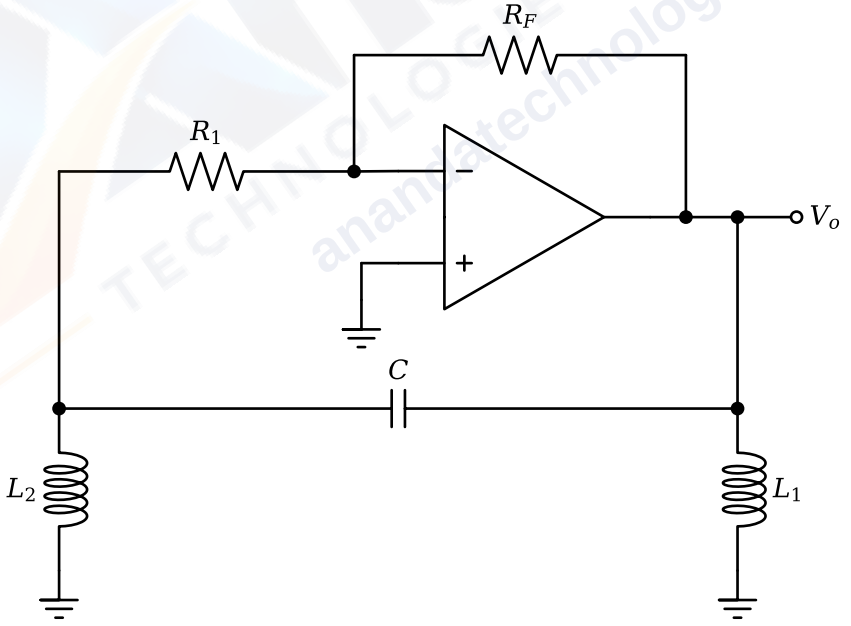


Waveforms of 555 monostable multivibrator

(Circuit 2 M, working 2 M, waveforms / pulse width 2 M)

c) Describe the working principle of Hartley oscillator using op-amp with circuit diagram. Derive the formula for its frequency of oscillation. 6 M

Circuit: The op-amp is an inverting amplifier (180° phase shift, gain $-R_F/R_1$). The tank circuit consists of two inductors L_1, L_2 (tapped coil) and one capacitor C. Element 1 is across the output, element 2 across the amplifier input side and element 3 between them; the tank gives another 180°, so total phase shift is 360°.



Hartley oscillator using op-amp

Working: At switch ON, noise starts oscillation in the tank circuit. The voltage across element 2 is fed back to the amplifier input through R_1; the amplifier supplies the energy lost in the tank so that the oscillations are sustained at the resonant frequency of the tank.

Derivation of frequency (general LC oscillator, amplifier output resistance R_o):

Let $X_1 = \omega L_1$, $X_2 = \omega L_2$, $X_3 = -1/(\omega C)$. The loop gain of the general LC oscillator is

$$\mathbf{A\beta = -A\,X_1X_2 \,/\, [\, jR_o(X_1 + X_2 + X_3) - X_1(X_2 + X_3)\,]}$$

For Aβ to be a real number (phase condition) the imaginary term must be zero:

$$\mathbf{X_1 + X_2 + X_3 = 0}$$

$\omega L_1 + \omega L_2 - 1/(\omega C) = 0 \Rightarrow \omega^2(L_1 + L_2)C = 1$

$$\mathbf{f_o = 1 \,/\, [2\pi \sqrt{((L_1 + L_2)\,C)}]}$$

(If mutual inductance M exists, $L_{eq} = L_1 + L_2 + 2M$.)

Using $X_2 + X_3 = -X_1$, the magnitude condition $|A\beta| = 1$ gives $|A| = X_1/X_2 = L_1/L_2 \Rightarrow R_F/R_1 \geq L_1/L_2$.

(Circuit 2 M, working 1 M, derivation 3 M)

Q.6 Attempt any TWO of the following: 12 marks

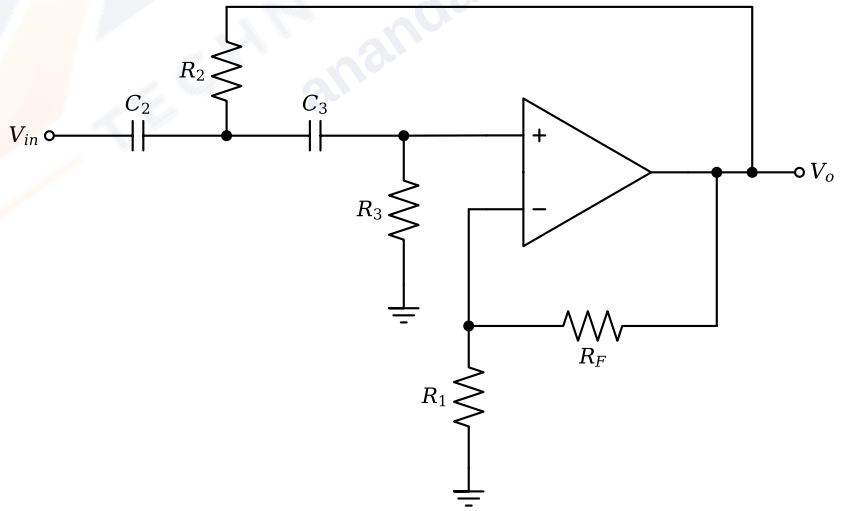
a) Design a second order Butterworth high pass filter with cut-off frequency 5 kHz. Draw the designed circuit and sketch its actual frequency response. (Assume C = 0.01 µF) 6 M

Given: f_L = 5 kHz. For a second order Butterworth response (Sallen-Key, equal components $R_2 = R_3 = R$, $C_2 = C_3 = C$), the pass band gain must be $A_F = 1.586$ (damping 0.707).

Step 1: $f_L = 1/(2\pi RC)$ (equal components). Choose C = 10 nF.

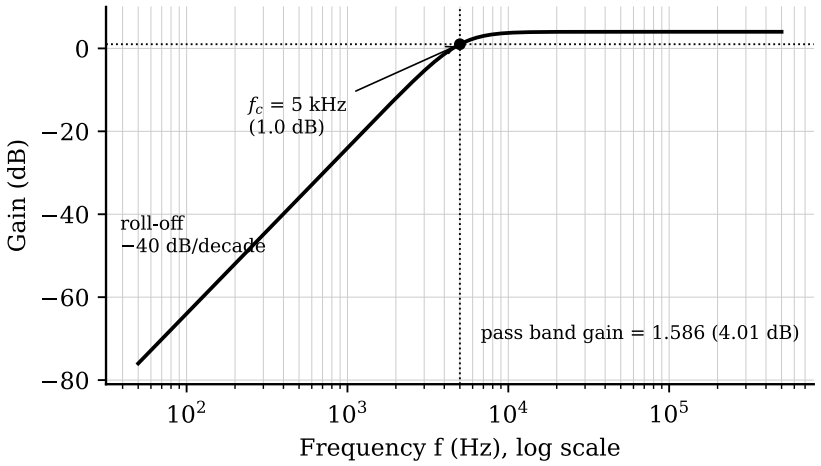
Step 2: $R = 1/(2\pi\, f_L\, C) = 1/(2\pi \times 5000 \times 10 \times 10^{-9})$ = **3.183 kΩ** → use 3.3 kΩ standard (f = 4.823 kHz) or a preset for exact value.

Step 3: $A_F = 1 + R_F/R_1 = 1.586 \Rightarrow R_F = 0.586\, R_1$. Choose R_1 = 10 kΩ ⇒ R_F = **5.86 kΩ** (use 5.6 kΩ + 270 Ω, or a 10 kΩ pot).



Designed second order Butterworth high pass filter

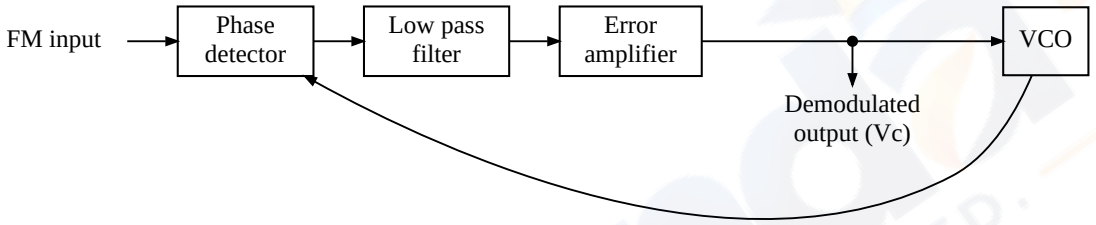
Component values: $R_2 = R_3$ = 3.3 kΩ, $C_2 = C_3$ = 10 nF, R_1 = 10 kΩ, R_F = 5.86 kΩ, op-amp IC 741 with ±15 V supply.



Actual frequency response: gain 1.586 (4.0 dB) in pass band, −3 dB at 5 kHz, roll-off 40 dB/decade

(Design 3 M, circuit 2 M, frequency response 1 M)

b) Explain the use of PLL as FM demodulator with the help of block diagram. 6 M



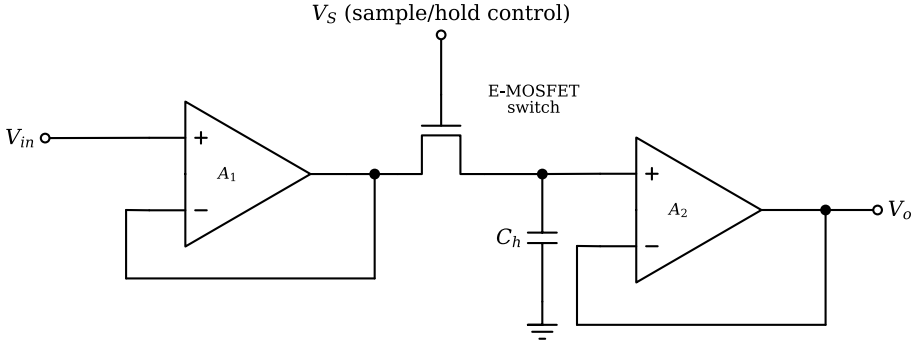
PLL as FM demodulator

Working:

- The FM signal is applied to the phase detector. The PLL locks to the FM carrier, and the VCO frequency follows the instantaneous frequency of the FM input.
- To make the VCO follow, the control voltage V_c at the VCO input must vary exactly as the frequency deviation of the FM signal.
- Since the frequency deviation is proportional to the modulating signal, V_c is the recovered (demodulated) audio signal. It is taken from the output of the error amplifier (after LPF).
- The PLL FM demodulator needs no tuned circuits and is linear; IC 565 is commonly used.

(Block diagram 3 M, working 3 M)

c) Draw and explain the sample and hold circuit using op-amp with input and output waveforms. 6 M

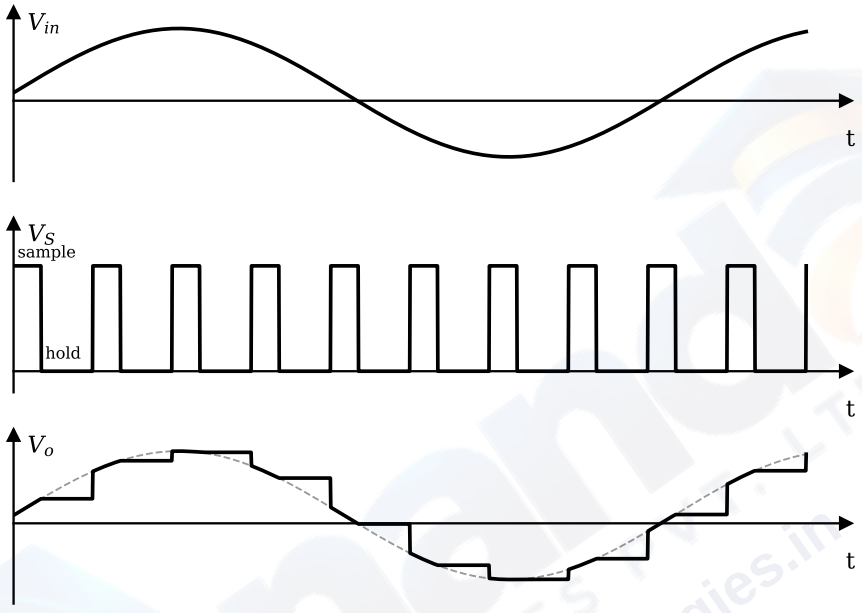


Sample and hold circuit using op-amp

Circuit: A_1 and A_2 are voltage followers. An E-MOSFET Q_1 works as a switch controlled by the sample/hold pulse V_S at its gate. A low-leakage capacitor C_h (polystyrene / mylar) stores the sampled voltage.

Working:

- **Sample period** (V_S HIGH): the MOSFET is ON; C_h charges quickly through the low output resistance of A_1 and its voltage follows V_{in}. $V_o = V_{in}$.
- **Hold period** (V_S LOW): the MOSFET is OFF; C_h is isolated and holds the last value of V_{in}. A_2 (very high input resistance) does not discharge C_h, so V_o stays constant.
- The output is therefore a staircase approximation of the input.



Sample and hold waveforms

Applications: analog-to-digital converters (input held constant during conversion), digital interfacing, pulse modulation systems, data distribution.

(Circuit 2 M, working 2 M, waveforms 2 M)

Note: This is a **model question paper prepared by Ananda Technologies** only for practice and exam preparation, based on the pattern of previous MSBTE question papers and the K-scheme syllabus. It is **not an official MSBTE paper**, and it does **not** mean that these questions will come in the exam. Answers follow standard textbook points; marks shown are indicative. Free for students — anandatechnologies.in