

Digital Techniques and Microprocessors (313305)

MSBTE K-Scheme · Information Technology (Sem III) · Important Questions

Based on MSBTE papers S-2024...S-2026 available on msbte.ac.in (papers analysed: W-24, S-25, W-25, S-26). Practice guidance only — not a prediction of the exam.

Probability: **High** = asked in 3 or 4 of the 4 papers · **Medium** = asked in 2 papers · **Low** = asked once, or in syllabus but not asked yet. Questions asked in different wording are grouped together.

Paper pattern (all 4 papers): Q1 any 5 of 7 (2 M) = 10; Q2 any 3 of 4 (4 M) = 12; Q3 any 3 of 4 (4 M) = 12; Q4 any 3 of 5 (4 M) = 12; Q5 any 2 of 3 (6 M) = 12; Q6 any 2 of 3 (6 M) = 12; total 70 marks, 3 hours.

Unit 1: Number Systems, Logic Gates and Boolean Algebra

Question / topic	Marks	Asked in (Q. no.)	Times	Probability
State and prove De Morgan's theorems	4, 6	S-26 (2a), W-25 (6a), S-25 (3d), W-24 (2a)	4	High
Number system conversions (decimal / binary / octal / hex), with steps	4	S-26 (3a), W-25 (3a), S-25 (2a)	3	High
Subtraction using 1's / 2's complement	4	W-25 (2a), S-25 (4a), W-24 (3a)	3	High
Symbol and truth table of logic gates (AND, NOR, NAND, EX-OR, EX-NOR)	2	S-26 (1f), W-25 (1a), W-24 (1f)	3	High
Boolean laws; reduce expression using Boolean laws	2, 6	S-26 (1a), W-25 (6a), S-25 (5a)	3	High
Define bit, nibble, byte, word	2	S-25 (1a), W-24 (1a)	2	Medium
Codes: hex to BCD rules, applications of Gray / ASCII code	2	S-26 (1b), W-25 (1c)	2	Medium
Basic gates using universal gates (NAND only / NOR only)	4	S-26 (4a), W-24 (4a)	2	Medium
BCD / hexadecimal addition	4	Not asked yet (syllabus)	0	Low

Unit 2: Combinational and Sequential Logic Circuits

Question / topic	Marks	Asked in (Q. no.)	Times	Probability
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K-map minimisation (SOP, don't care, POS, NAND-NAND) with logic diagram	4, 6	S-26 (3b), W-25 (4e/5c), S-25 (2b), W-24 (3b)	5	High
Multiplexer / demultiplexer (8:1 MUX, 16:1 using 8:1, 1:4 DEMUX, MUX vs DEMUX)	2, 4, 6	S-26 (2b/4b), W-25 (1b), W-24 (5a)	4	High
Half adder / half subtractor design	4	W-25 (2b), S-25 (4b), W-24 (2b)	3	High
Minterm / maxterm; canonical (standard) SOP and POS forms	2, 4	W-25 (4a), S-25 (1b/3a)	3	Medium
Combinational vs sequential circuit; short notes on clock, latch, flip-flop, counter	4, 6	S-26 (6a), W-24 (4b/6a)	3	Medium
Applications of flip-flop / latch / counter / buffer	2, 4	W-25 (3b), S-25 (1f)	2	Medium
J-K flip-flop logic diagram and truth table	6	S-26 (5b)	1	Low
Find output (truth table) of a given logic circuit	6	S-25 (6a)	1	Low
Full adder, SR / D / T flip-flops, counters (syllabus, not asked yet)	—	Not asked yet (syllabus)	0	Low

Unit 3: 16-bit Microprocessor 8086

Question / topic	Marks	Asked in (Q. no.)	Times	Probability
Memory segmentation in 8086	4, 6	S-26 (2c), W-25 (4c), S-25 (5b)	3	High
Physical address calculation / generation	4, 6	W-25 (6c), S-25 (5b), W-24 (2c)	3	High
Architecture of 8086; functions of BIU and EU	4, 6	S-26 (4c), W-24 (5b)	2	Medium
Pipelining in 8086 (concept / advantages)	2, 6	S-26 (1c), W-25 (6c)	2	Medium
Flag register of 8086	2, 4	S-25 (1c), W-24 (4c)	2	Medium
Functions of 8086 pins (ALE, DT/R, RD, READY, M/IO, HOLD ...)	2, 4	W-25 (1g), S-25 (4c)	2	Medium
Minimum mode configuration of 8086	4, 6	S-26 (5a), S-25 (2c)	2	Medium
Features / applications of 8086	2	W-24 (1b/1c)	2	Low

Minimum vs maximum mode	4	W-25 (3c)	1	Low
Use of index registers, BP, IP (register organisation)	2	W-25 (1f)	1	Low
Pin diagram of 8086; timing diagram concept (syllabus, not asked yet)	—	Not asked yet (syllabus)	0	Low

Unit 4: 8086 Instruction Set, Addressing Modes and Directives

Question / topic	Marks	Asked in (Q. no.)	Times	Probability
Addressing modes of 8086 (list / explain with examples)	2, 4, 6	S-26 (3c), W-25 (5b), S-25 (4d), W-24 (1d/3c)	5	High
Write instruction(s) for given operations (MUL, IDIV, ROL, SHR, AND, load segment / stack)	4, 6	S-26 (6b), W-25 (2d/4b), S-25 (6b)	4	High
Assembler directives (DB, DW, DD, DQ, ASSUME, EQU ...)	2	W-25 (1d), S-25 (1d), W-24 (1g)	3	High
String instructions (MOVSB, CMPSW, REP ...)	4	S-26 (3d), S-25 (3b), W-24 (4d)	3	High
Arithmetic / any instructions with format and example	2	S-26 (1g), S-25 (1g), W-24 (1e)	3	High
DAA / AAA / PUSH / IDIV / XOR — explain instruction	2, 4	W-25 (1e/4d), S-25 (2d)	3	Medium
Shift and rotate instructions	4	W-25 (3d), W-24 (3d)	2	Medium
Predict register / flag contents after given instructions	4, 6	W-25 (2c), W-24 (6b)	2	Medium
Flag manipulation instructions (STC, CLC, CMC, STD, CLD ...)	2, 4	S-26 (4d), W-25 (1e)	2	Medium
Identify addressing mode of given instructions	6	S-25 (5c)	1	Low
Assembler and linker (programming tools)	2	S-26 (1d)	1	Low

Unit 5: Assembly Language Programming using 8086

Question / topic	Marks	Asked in (Q. no.)	Times	Probability
ALP: add / subtract / multiply two numbers (8-bit, 16-bit, hex)	2, 4	S-26 (2d), S-25 (1e), W-24 (2d)	3	High
ALP: sort array in ascending / descending order with flowchart	6	S-26 (5c), W-25 (5a), W-24 (6c)	3	High

ALP: smallest / largest number in array	4, 6	S-25 (3c), W-24 (5c)	2	Medium
ALP: sum of series / sum of BCD numbers in array	4, 6	W-25 (6b), W-24 (4e)	2	Medium
ALP on strings: block transfer, concatenation (string length / reverse / compare)	4, 6	S-26 (4e), S-25 (6c)	2	Medium
ALP: count occurrence of a number (even / odd, positive / negative count)	4	S-25 (4e)	1	Low
ALP: BCD multiplication with flowchart	6	S-26 (6c)	1	Low
ALP using branching instructions (any)	2	S-26 (1e)	1	Low

Top repeated topics (all units)

1. K-map minimisation (SOP, don't care, POS, NAND-NAND) with logic diagram — in 4 of 4 papers (5 times)
2. Addressing modes of 8086 (list / explain with examples) — in 4 of 4 papers (5 times)
3. State and prove De Morgan's theorems — in 4 of 4 papers (4 times)
4. Multiplexer / demultiplexer (8:1 MUX, 16:1 using 8:1, 1:4 DEMUX, MUX vs DEMUX) — in 3 of 4 papers (4 times)
5. Write instruction(s) for given operations (MUL, IDIV, ROL, SHR, AND, load segment / stack) — in 3 of 4 papers (4 times)
6. Number system conversions (decimal / binary / octal / hex), with steps — in 3 of 4 papers (3 times)
7. Subtraction using 1's / 2's complement — in 3 of 4 papers (3 times)
8. Symbol and truth table of logic gates (AND, NOR, NAND, EX-OR, EX-NOR) — in 3 of 4 papers (3 times)
9. Boolean laws; reduce expression using Boolean laws — in 3 of 4 papers (3 times)
10. Half adder / half subtractor design — in 3 of 4 papers (3 times)

How to use: prepare every High topic fully (diagram + table + example), then Medium topics. Numericals (conversions, K-maps, complements, physical address) and programs (ALPs) come with new values every time — practise the method and the program logic, not the exact answer.

Note: This is a **important-questions list prepared by Ananda Technologies** only for practice and exam preparation, based on the pattern of previous MSBTE question papers and the K-scheme syllabus. It is **not an official MSBTE paper**, and it does **not** mean that these questions will come in the exam. Answers follow standard textbook points; marks shown are indicative. Free for students — anandatechnologies.in